SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

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Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF MECHATRONICS ENGINEERING

19MCT201 - DESIGN OF DIGITAL CIRCUITS

II YEAR - III SEM

UNIT 3 – SEQUENTIAL CIRCUITS

TOPIC 7 & 8 – Up/ Down Counter

SEQUENTIAL CIRCUITS

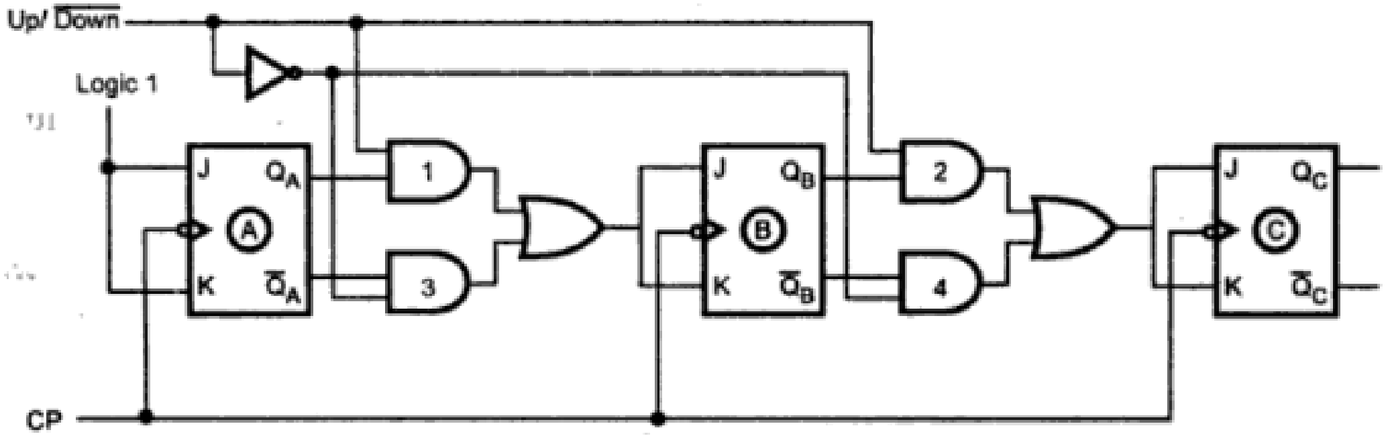
Latches, Edge triggered Flip flops SR, JK, T, D and Master slave – Characteristic table and equation, Application table, Synchronous counters, Design of synchronous counters, up/down counter, Modulo–n counter, Decade counters. Design of Sequential circuits using simulation

Up/ Down Counter

- An up-counter counts events in increasing order
- A down-counter counts stuff in the decreasing order
- An up-down counter is a combination of an up-counter and a down-counter. It can count in both directions, increasing as well as decreasing.

Up/ Down Counter

CP	UP	Q_C	Q_B	Q_A	DOWN
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	



3-bit synchronous/parallel up/down counter

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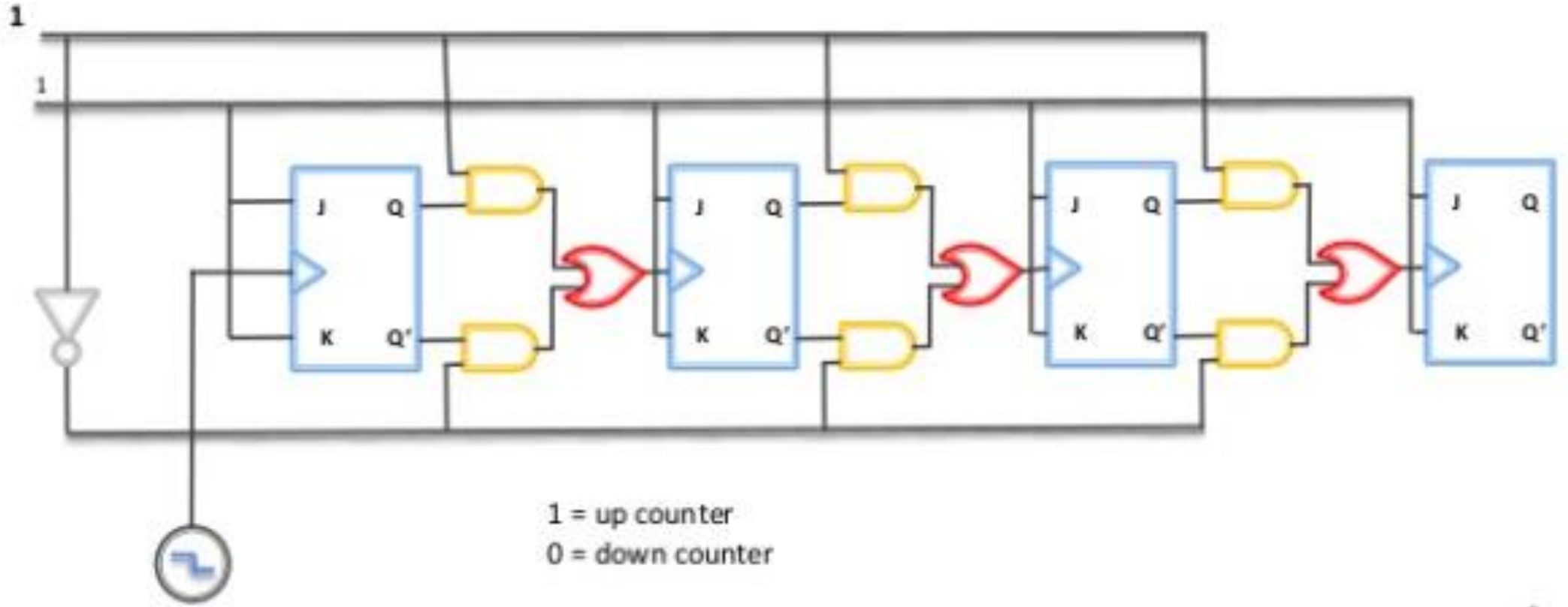
Up/ Down Counter



Up/ Down Counter

Step 4 : K-map simplification for flip-flop inputs.

For J_A

Q_A \ Q_BQ_C	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$J_A = Q_B Q_C$

For K_A

Q_A \ Q_BQ_C	00	01	11	10
0	X	X	X	X
1	0	1	X	X

$K_A = Q_C$

For J_B

Q_A \ Q_BQ_C	00	01	11	10
0	0	1	X	X
1	0	0	X	X

$J_B = \overline{Q}_A Q_C$

For K_B

Q_A \ Q_BQ_C	00	01	11	10
0	X	X	1	0
1	X	X	X	X

$K_B = Q_C$

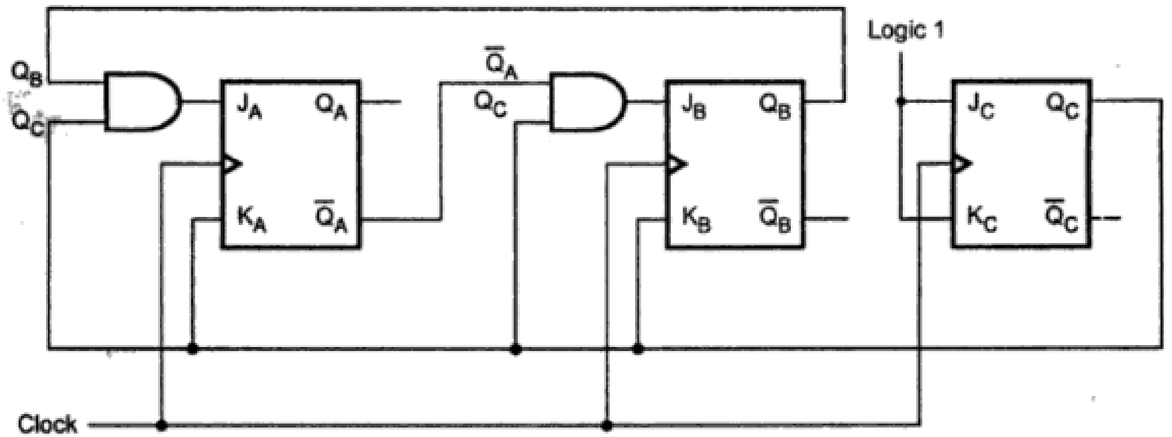
For J_C

Q_A \ Q_BQ_C	00	01	11	10
0	1	X	X	1
1	1	X	X	X

For K_C

Q_A \ Q_BQ_C	00	01	11	10
0	X	1	1	X
1	X	1	X	X

Step 5 : Implement the counter.



Up/ Down Counter

Design of a Synchronous Mod-6 Counter using Clocked JK Flip-Flops

Step 1 : Find number of flip-flops required to build the counter :

Flip-Flops required are : $2^n \geq N$.

Here $N = 6 \quad \therefore \; n = 3$

i.e. three flip-flops are required.

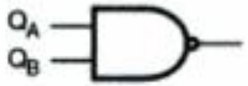
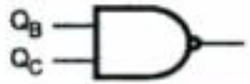
Step 2 : Write an excitation table for JK flip-flop.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step 3 : Determine the transition table.

Present state			Next state			Flip-flop inputs					
Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	0	0	0	x	1	0	x	x	1
1	1	0	x	x	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x	x	x

MoD Counter

NAND Gate Inputs	Counter
	MOD-1 Counter
	MOD-2 Counter
	MOD-3 Counter
	MOD-4 Counter
	MOD-5 Counter
	MOD-6 Counter
	MOD-7 Counter

NAND gate inputs for MOD-n counter

ASSESSMENT - 1

Mux relates with us….

Question 1

Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?

- a) Data Selector
- b) Data distributor
- c) Both data selector and data distributor
- d) DeMultiplexer

Question 2

Which is the major functioning responsibility of the multiplexing combinational circuit?

- a) Decoding the binary information
- b) Generation of all minterms in an output function with OR-gate
- c) Generation of selected path between multiple sources and a single destination
- d) Encoding of binary information

References

- https://brilliant.org/wiki/de-morgans-laws/
- https://circuitglobe.com/demorgans-theorem.html
- https://www.electrical4u.com/