

SNS COLLEGE OF TECHNOLOGY

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DEPARTMENT OF MECHATRONICS ENGINEERING

19MCT201 - DESIGN OF DIGITAL CIRCUITS II YEAR - III SEM

UNIT 3 – SEQUENTIAL CIRCUITS

TOPIC 2 – Counter







SEQUENTIAL CIRCUITS

Latches, Edge triggered Flip flops SR, JK, T, D and Master slave – Characteristic table and equation, Application table, Synchronous counters, Design of synchronous counters, up/down counter, Modulo-n counter, Decade counters. Design of Sequential circuits using simulation







Flip flops

FLIP-FLOP NAME	FLIP-FLOP SYMBOL	CHARACTERISTIC TABLE	CHARACTERISTIC EQUATION	EXCITATION TABLE		
SR	SQ 	S R Q(next) 0 0 Q 0 1 0 1 0 1 1 1 ?	$\mathbf{Q}_{(next)} = \mathbf{S} + \mathbf{R'Q}$ $\mathbf{SR} = 0$	Q 0 1 1	Q(next) 0 1 0 1 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0	S R 0 X 1 0 0 1 X 0
JK	— J Q —>сік — К Q'	J K Q(next) 0 0 Q 0 1 0 1 0 1 1 1 Q'	$\mathbf{Q}_{(next)} = \mathbf{J}\mathbf{Q}' + \mathbf{K'}\mathbf{Q}$	Q 0 1 1	Q(next) 0 1 0 1 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0	J K 0 X 1 X X 1 X 0
D	— D Q — >Cik — Q'	D Q(next) 0 0 1 1	$\mathbf{Q}_{(next)} = \mathbf{D}$	Q 0 0 1 1	Q(next) 0 1 0 1 0 1 0 1	D 0 1 0 1 0 1
Т	──TQ ──>CIk Q'	T Q(next) 0 Q 1 Q'	$\mathbf{Q}_{(next)} = \mathbf{T}\mathbf{Q'} + \mathbf{T'}\mathbf{Q}$	Q 0 0 1 1	Q(next) 0 1 0 1 0	T 0 1 1 0



The Master-Slave JK Flip Flop





The circuit accepts input data when the clock signal is "HIGH", and passes the data to the output on the falling-edge of the clock signal. In other words, the Master-Slave JK Flip flop is a "Synchronous" device as it only passes data with the timing of the clock signal.



The input signals J and K are connected to the gated "master" SR flip flop which "locks" the input condition while the clock (Clk) input is "HIGH" at logic level "1". As the clock input of the "slave" flip flop is the inverse (complement) of the "master" clock input, the "slave" SR flip flop does not toggle. The outputs from the "master" flip flop are only "seen" by the gated "slave" flip flop when the clock input goes "LOW" to logic level "0".

When the clock is "LOW", the outputs from the "master" flip flop are latched and any additional changes to its inputs are ignored. The gated "slave" flip flop now responds to the state of its inputs passed over by the "master" section.



Counters

A counter is a register capable of counting the number of clock pulses arriving at its clock input. Count represents the number of clock pulses arrived. A specified sequence of states appears as the counter output. This is the main difference between a register and a counter. A specified sequence of states is different for different types of counters.

There are two types of counters, synchronous and asynchronous.



A two-bit asynchronous binary counter



Counters



Design of Synchronous Counter

- Obtain the transition table from the given circuit information.
- Determine the number of flip-flops needed.
- Choose the type of flip-flops to be used.
- From the transition table, derive the circuit excitation table. ا ا ا ا
 - 5. Use K-map or any other simplification method to derive the circuit the flip-flop input functions.
 - Draw the logic diagram.



Design of a Synchronous Mod-6 Counter using Clocked JK Flip-Flops

Step 1 : Find number of flip-flops required to build the counter :

Flip-Flops required are $: 2^n \ge N$.

Here N = 6 \therefore n = 3

i.e. three flip-flops are required.

Step 2 : Write an excitation table for JK flip-flop.

Qn	Q _{n+1}	J	к
0	0	0	х
0	1	1	x
1	0	х	1
1	1	х	0

Present state			M	lext stat	e	Flip-flop inputs					
Q _A	QB	Qc	QA+1	Q _{B +1}	Q _{C +1}	JA	KA	JB	KB	Jc	Kc
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	×
1	0	1	0	0	0	x	1	0	x	x	1
1	1	0	x	x	x	x	x	x	x	x	×
1	1	1	x	x	x	x	x	x	x	x	x



6/16/2020

Counters





Counters

Design of a Synchronous Mod-6 Counter using Clocked JK Flip-Flops

Step 4 : K-map simplification for flip-flop inputs.

ͺ Q _B	Q _C	Fo	r J _A				
¢٨	00	01	11	10			
0	0	0	3	0			
1	х	х	\otimes	х			
J _A = Q _B Q _C							



Step 5 : Implement the counter.















ASSESSMENT - 1

Mux relates with us....

Question 1 Which combinational circuit is renowned for selecting a single Which is the major functioning responsibility of the input from multiple inputs & directing the binary information multiplexing combinational circuit? to output line? ▶ a) Data Selector a) Decoding the binary information ▶ b) Data distributor **b**) Generation of all minterms in an output function with OR-gate **c**) Both data selector and data distributor **c**) Generation of selected path between multiple sources and a single destination ▶ d) DeMultiplexer d) Encoding of binary information MULTIPLEXER/DESIGN OF DIGITAL CIRCUITS/R.YASODHARAN/MCT/SNSCT 6/16/2020



Question 2



References

- <u>https://brilliant.org/wiki/de-morgans-laws/</u>
- <u>https://circuitglobe.com/demorgans-theorem.html</u>
- https://www.electrical4u.com/ ullet

