SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A+' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF MECHATRONICS ENGINEERING

19MCT201 - DESIGN OF DIGITAL CIRCUITS

II YEAR - III SEM

UNIT 5 – DIGITAL LOGIC FAMILIES AND PLD

TOPIC 3– RAM

RAM

Random Access Memory (RAM) is a volatile memory and loses all its data when the power is switched off. It is the main memory of the computer system that stores the data temporarily and allows the data to be accessed in any order.

- ✓ Can be both read and written
- ✓ Is volatile
- ✓ Can be used only as temporary storage
- ✓ Two forms:
  - dynamic

data tend to decay even with power continuously applied

  - static

data are held as long as power is supplied

RAM

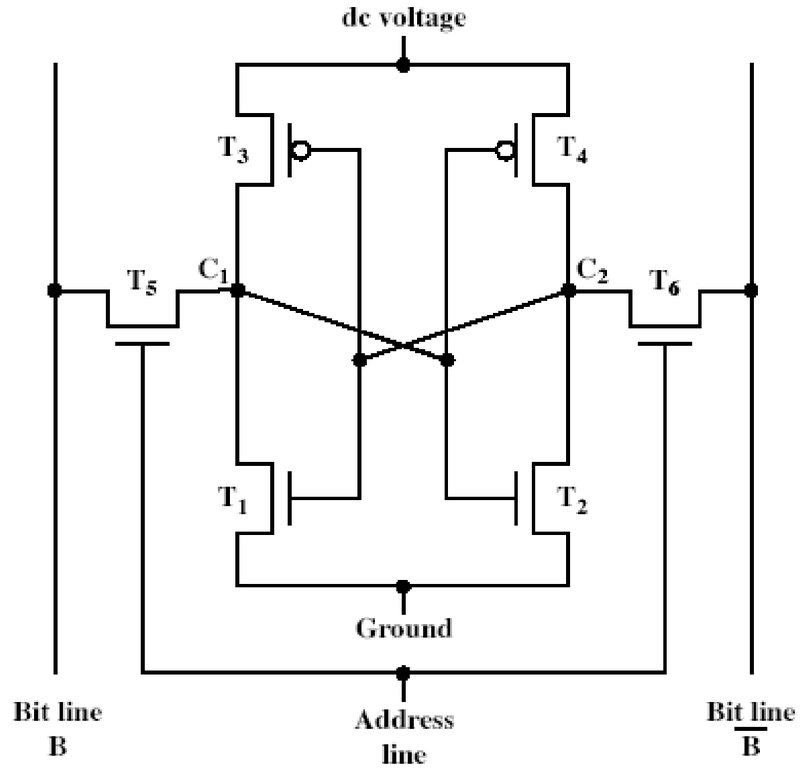
The RAM family includes two important memory devices: static RAM (SRAM) and dynamic RAM (DRAM). The primary difference between them is the lifetime of the data they store.

1) SRAM retains its contents as long as electrical power is applied to the chip. If the power is turned off or lost temporarily, its contents will be lost forever.
2) DRAM, on the other hand, has an extremely short data lifetime-typically about four milliseconds. This is true even when power is applied constantly. DRAM controller is used to refresh the data before it expires, the contents of memory can be kept alive for as long as they are needed. So DRAM is as useful as SRAM after all.

Static RAM (SRAM)

- Data stored as a combination of transistors' on-off
  - T1, T4 off, T2, T3 on: 1
  - T1, T4 on, T2, T3 off: 0
- Data are held as long as power is supplied, no refresh is needed

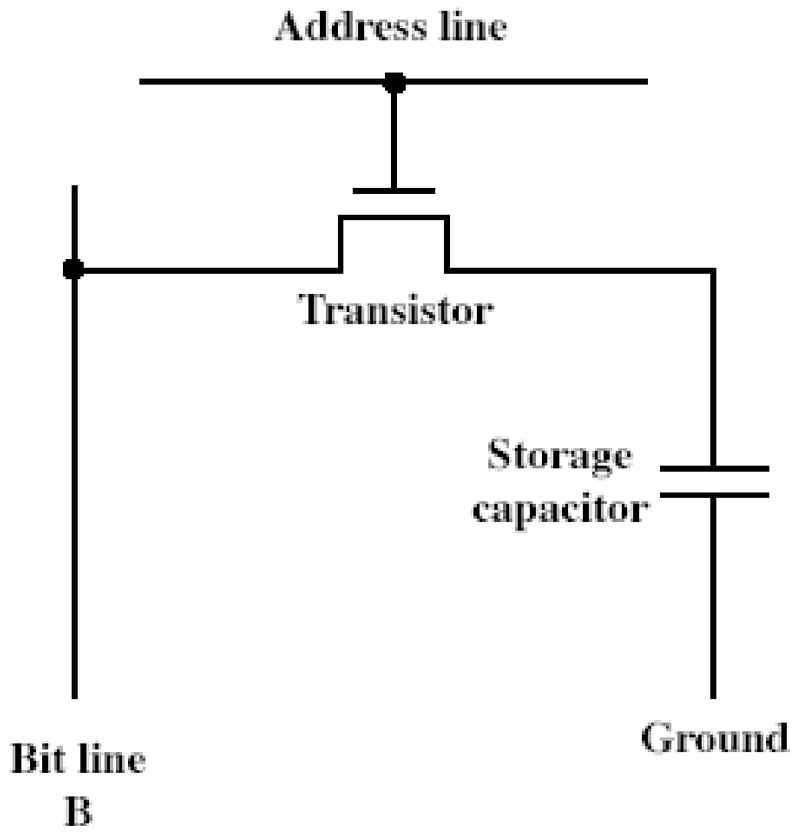
- A SRAM cell:



Dynamic RAM (DRAM)

- Data stored as charge on capacitors
  - presence: 1
  - absence: 0
  - threshold
- Need charge refreshing to maintain data storage

- A DRAM cell:



DRAM *vs.* SRAM

Volatile, Read-Write

- DRAM cell
  - Refresh needed
  - Smaller and simpler
  - More dense
  - Less expensive
  - For main memory
- SRAM cell
  - No refresh
  - Faster
  - For cache memory

ASSESSMENT - 1

Mux relates with us….

Question 1

Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?

- a) Data Selector
- b) Data distributor
- c) Both data selector and data distributor
- d) DeMultiplexer

Question 2

Which is the major functioning responsibility of the multiplexing combinational circuit?

- a) Decoding the binary information
- b) Generation of all minterms in an output function with OR-gate
- c) Generation of selected path between multiple sources and a single destination
- d) Encoding of binary information

References

- https://brilliant.org/wiki/de-morgans-laws/
- https://circuitglobe.com/demorgans-theorem.html
- https://www.electrical4u.com/