



SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution



Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A+' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF MECHATRONICS ENGINEERING

19MCT201 - DESIGN OF DIGITAL CIRCUITS

II YEAR - III SEM

UNIT 5 – DIGITAL LOGIC FAMILIES AND PLD

TOPIC 3– RAM



Why Programmable Logic Devices?



- Facts:
 - It is most economical to produce an IC in large volumes
 - Many designs required only small volumes of ICs
- Need an IC that can be:
 - Produced in large volumes
 - Handle many designs required in small volumes
- A programmable logic part can be:
 - made in large volumes
 - programmed to implement large numbers of different low-volume designs
- Many programmable logic devices are *field-programmable*, i. e., can be programmed outside of the manufacturing environment
- Most programmable logic devices are *erasable* and *reprogrammable*.
 - Allows “updating” a device or correction of errors
 - Allows reuse the device for a different design - the ultimate in re-usability!
 - Ideal for course laboratories
- Programmable logic devices can be used to prototype design that will be implemented for sale in regular ICs.
 - Complete Intel Pentium designs were actually prototype with specialized systems based on large numbers of VLSI programmable devices!



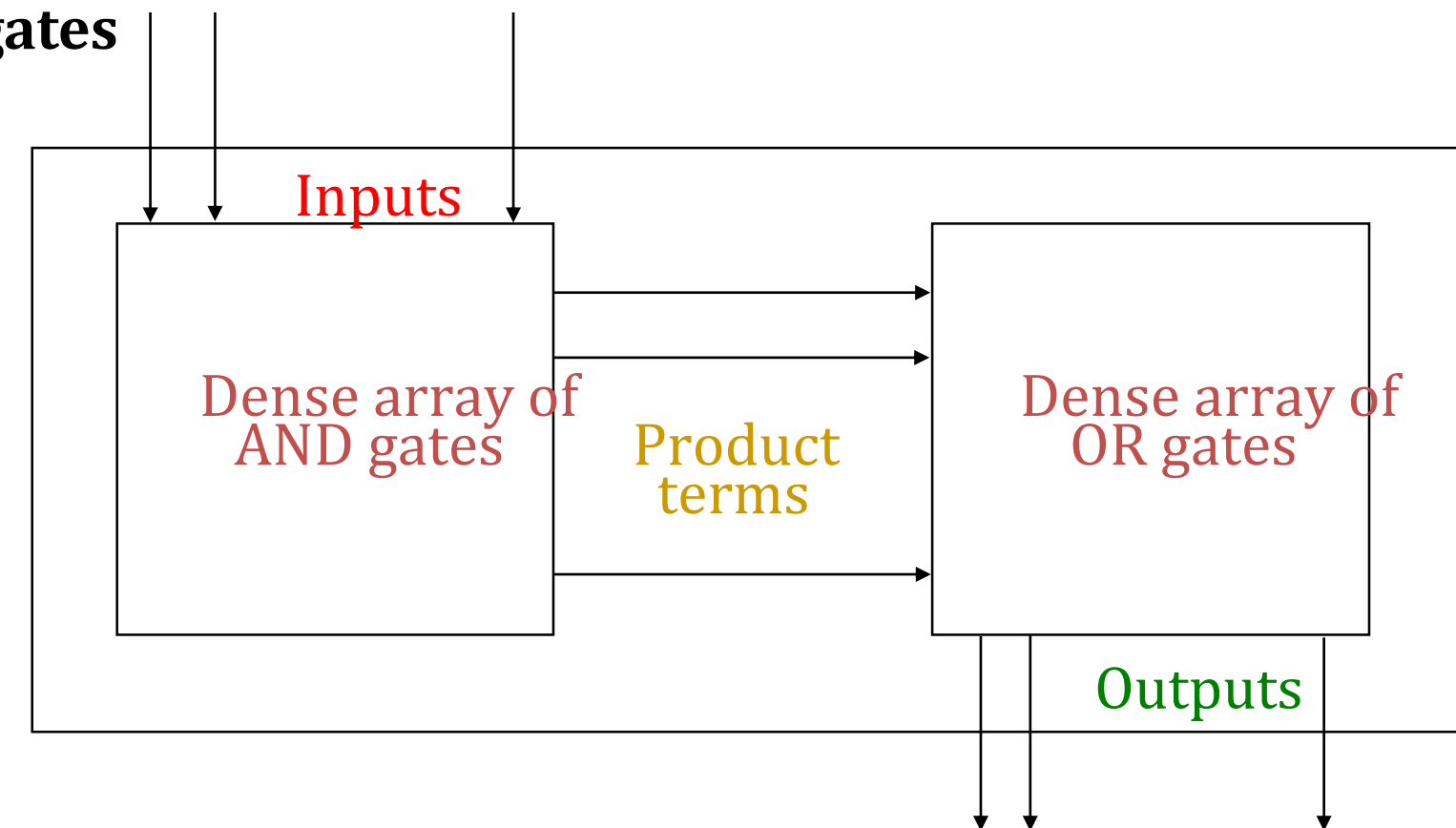
Types of PLD

- The purpose of a PLD device is to permit elaborate digital logic designs to be implemented by the user in a single device.
- Can be erased electrically and reprogrammed with a new design, making them very well suited for academic and prototyping

- **Pre-fabricated building block of many AND/OR gates (or NOR, NAND)**
- **"Personalized" by making or breaking connections among the gates**

• *Types of Programmable Logic Devices*

- SPLDs (Simple Programmable Logic Devices)
 - PROM (Programmable Read-Only Memory)
 - PLA (Programmable Logic Array)
 - PAL (Programmable Array Logic)
 - GAL (Generic Array Logic)
- CPLD (Complex Programmable Logic Device)
- FPGA (Field-Programmable Gate Array)

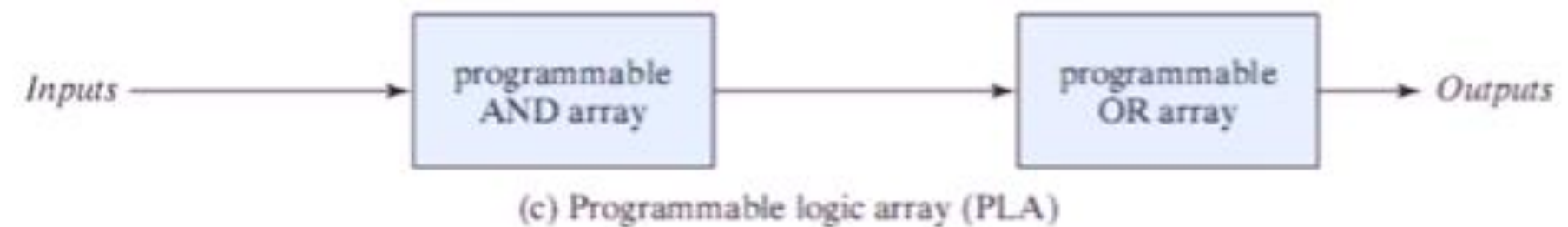
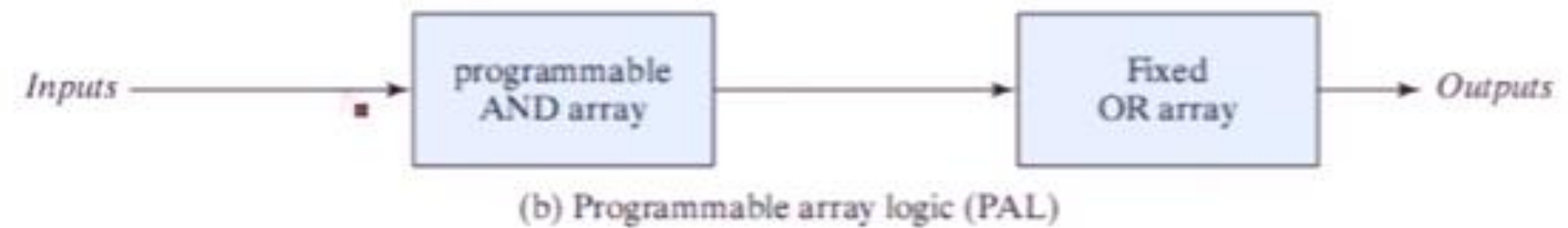
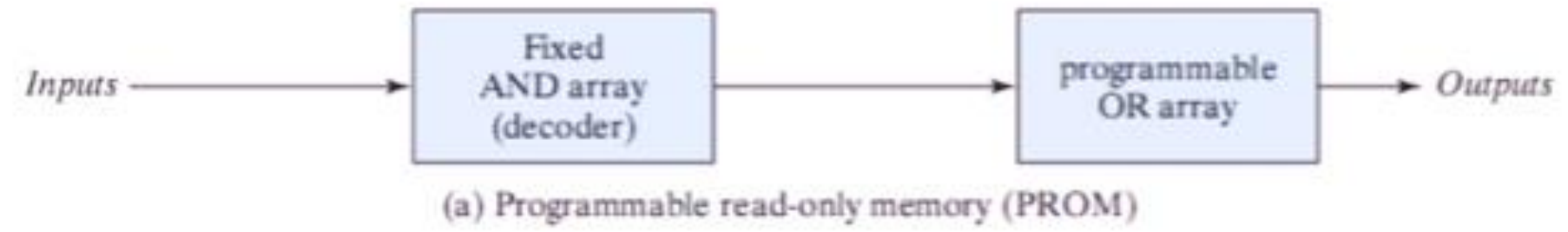




Types of PLD

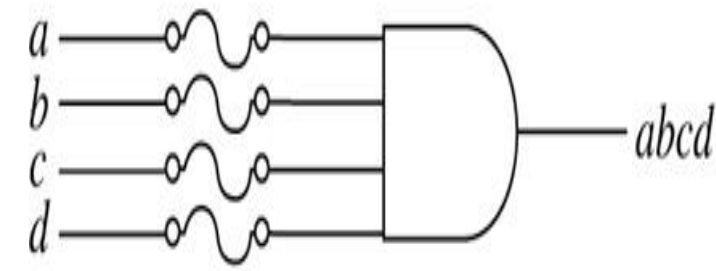
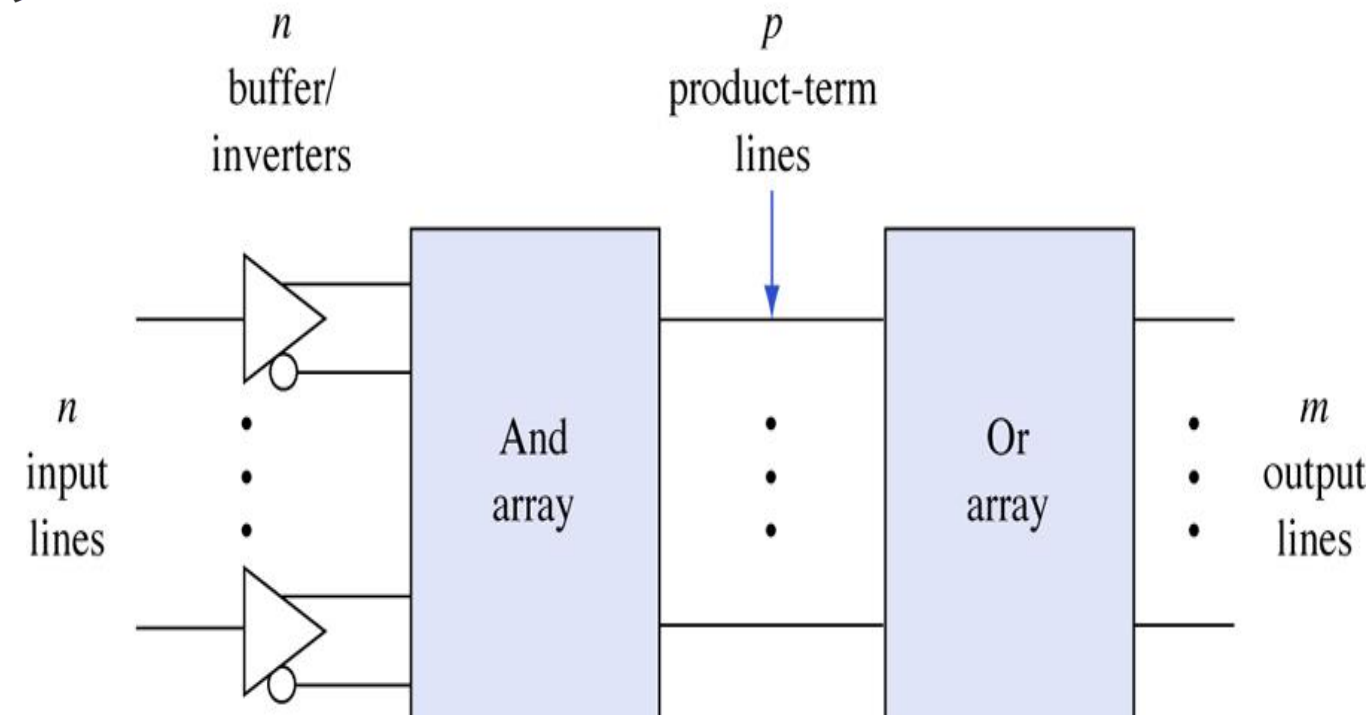


- The differences between the first three categories are these:
 - In a ROM, the input connection matrix is hardwired. The user can modify the output connection matrix.
 - In a PAL/GAL the output connection matrix is hardwired. The user can modify the input connection matrix.
 - In a PLA the user can modify both the input connection matrix and the output connection matrix.



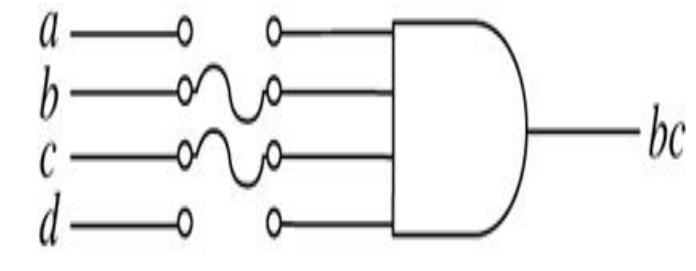


Dynamic RAM (DRAM)



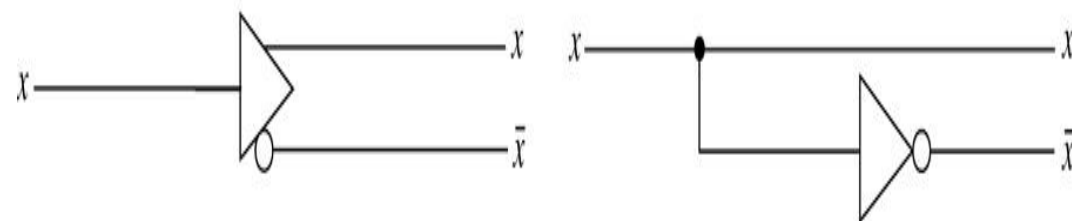
(a)

(a) Before programming.



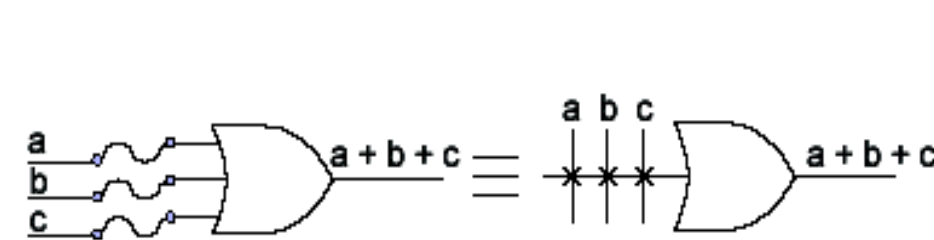
(b)

(b) After programming.

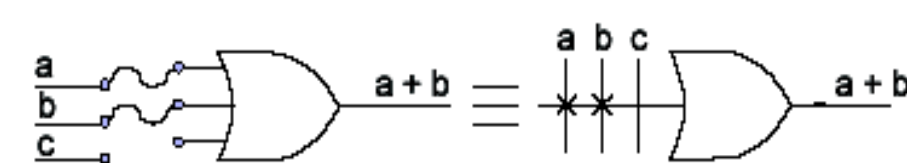


(a)

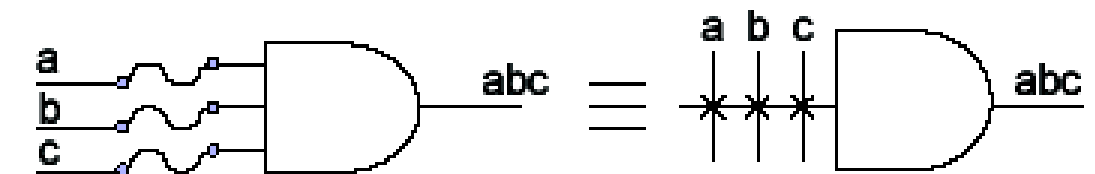
(b)



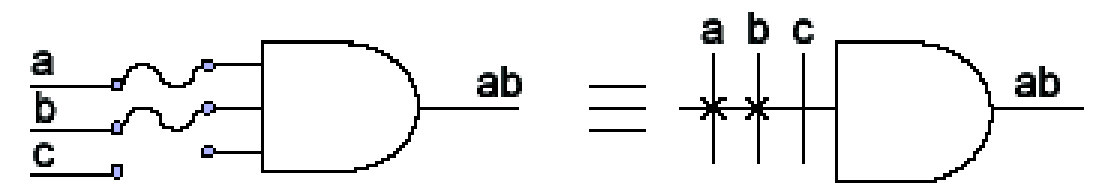
OR gate before programming



OR gate after programming



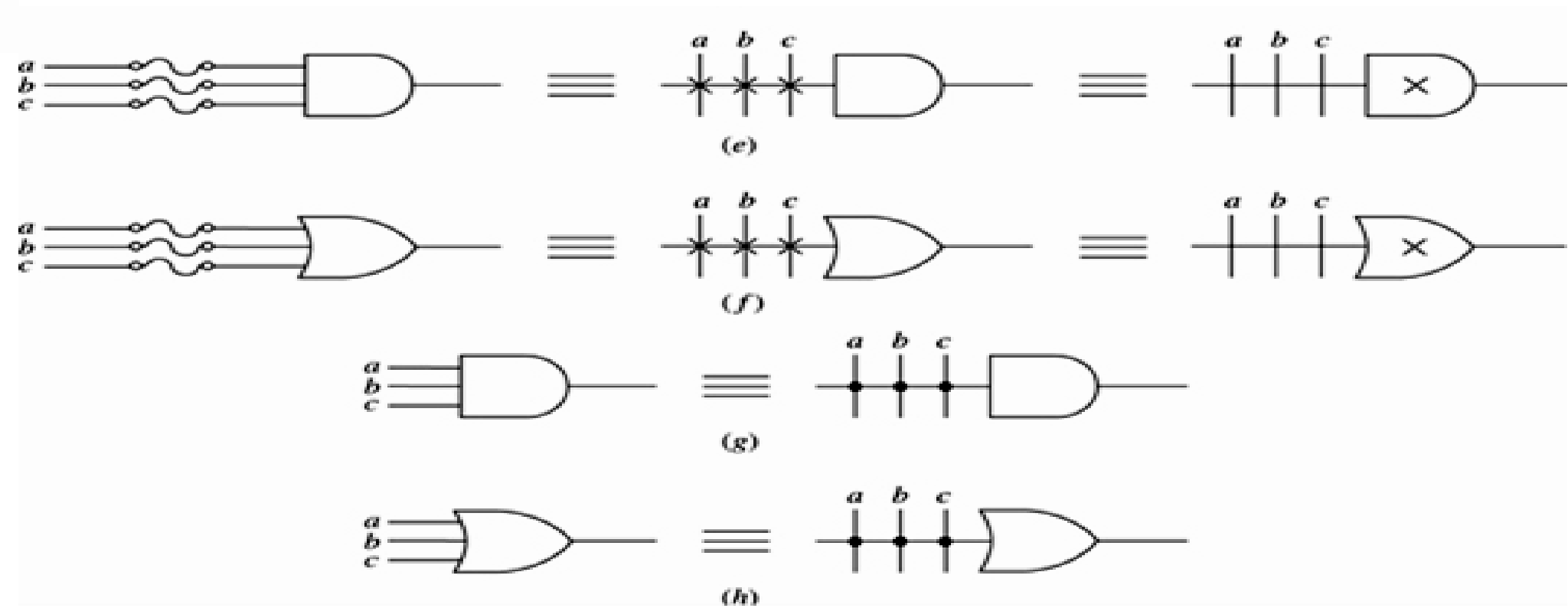
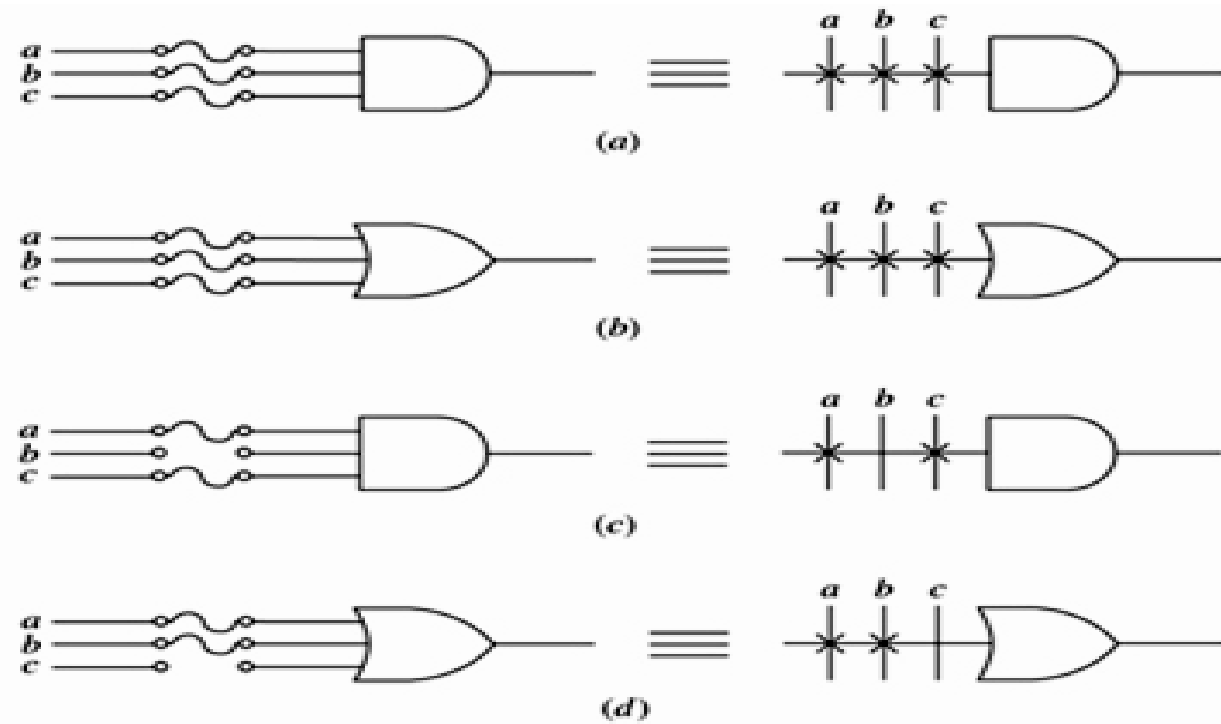
AND gate before programming



AND gate after programming



PLD Programming





ASSESSMENT - 1

Mux relates with us....

Question 1

Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?

- ▶ a) Data Selector
- ▶ b) Data distributor
- ▶ c) Both data selector and data distributor
- ▶ d) DeMultiplexer

Question 2

Which is the major functioning responsibility of the multiplexing combinational circuit?

- ▶ a) Decoding the binary information
- ▶ b) Generation of all minterms in an output function with OR-gate
- ▶ c) Generation of selected path between multiple sources and a single destination
- ▶ d) Encoding of binary information



References

- <https://brilliant.org/wiki/de-morgans-laws/>
- <https://circuitglobe.com/demorgans-theorem.html>
- <https://www.electrical4u.com/>