SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
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DEPARTMENT OF MECHATRONICS ENGINEERING

19MCT201 - DESIGN OF DIGITAL CIRCUITS

II YEAR - III SEM

UNIT 5 – DIGITAL LOGIC FAMILIES AND PLD

TOPIC 7– Logic Families

Logic Families

Logic Families indicate the type of logic circuit used in the IC. The main types of logic families are:

- TTL(Transistor Transistor Logic)
- CMOS (Complementary MOS)
- ECL (Emitter Coupled Logic)

Characteristics of Logic Families

The main characteristics of Logic families include:

- Speed
- Fan-in
- Fan-out
- Noise Immunity
- Power Dissipation

Speed: Speed of a logic circuit is determined by the time between the application of input and change in the output of the circuit.

Fan-in: It determines the number of inputs the logic gate can handle.

Fan-out: Determines the number of circuits that a gate can drive.

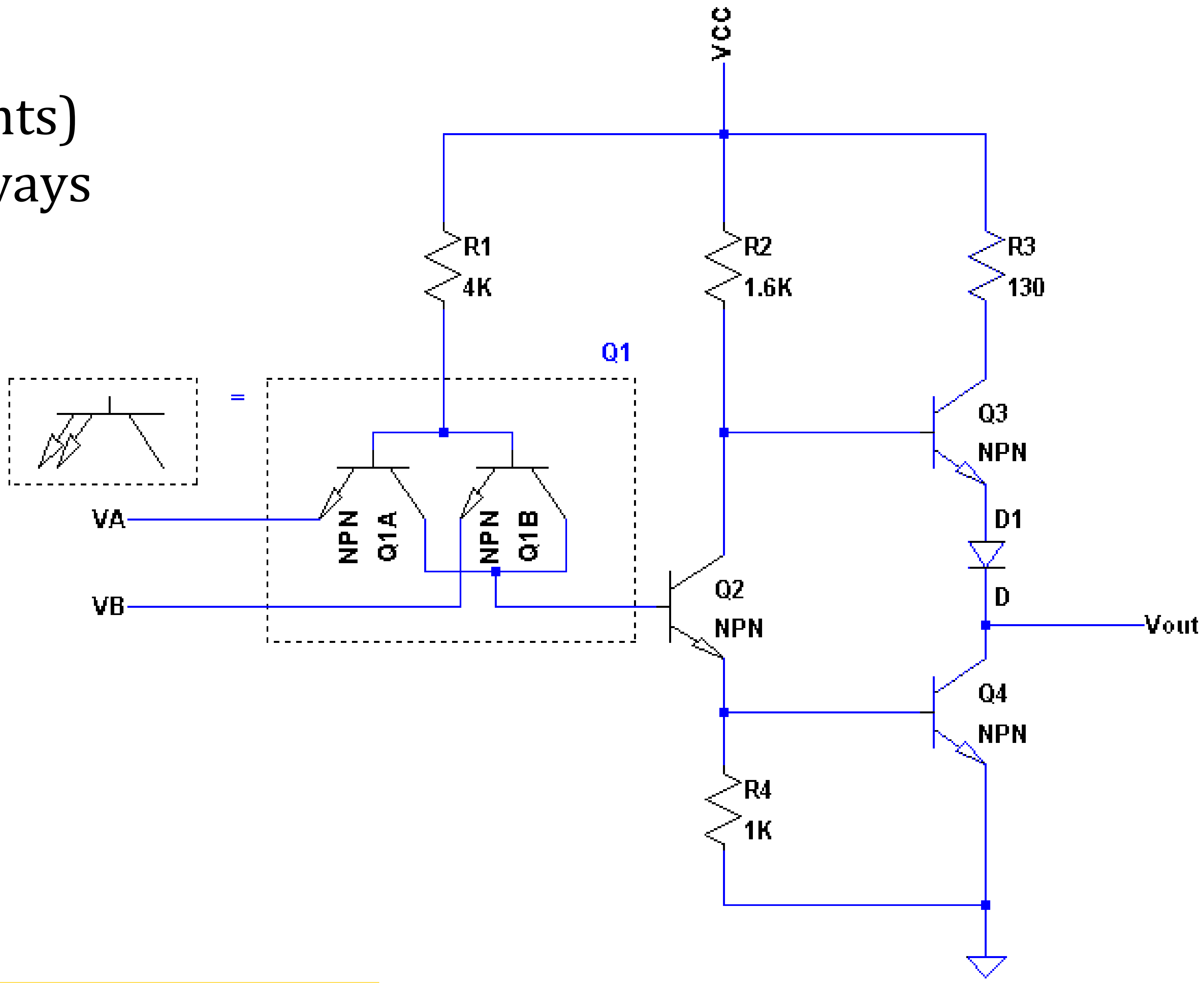
Noise Immunity: Maximum noise that a circuit can withstand without affecting the output.

Power: When a circuit switches from one state to the other, power dissipates.

TTL

Bipolar Transistor-Transistor Logic (TTL)

- first introduced by in 1964 (Texas Instruments)
- TTL has shaped digital technology in many ways
- Standard TTL family (e.g. 7400) is obsolete
- Newer TTL families still used (e.g. 74ALS00)



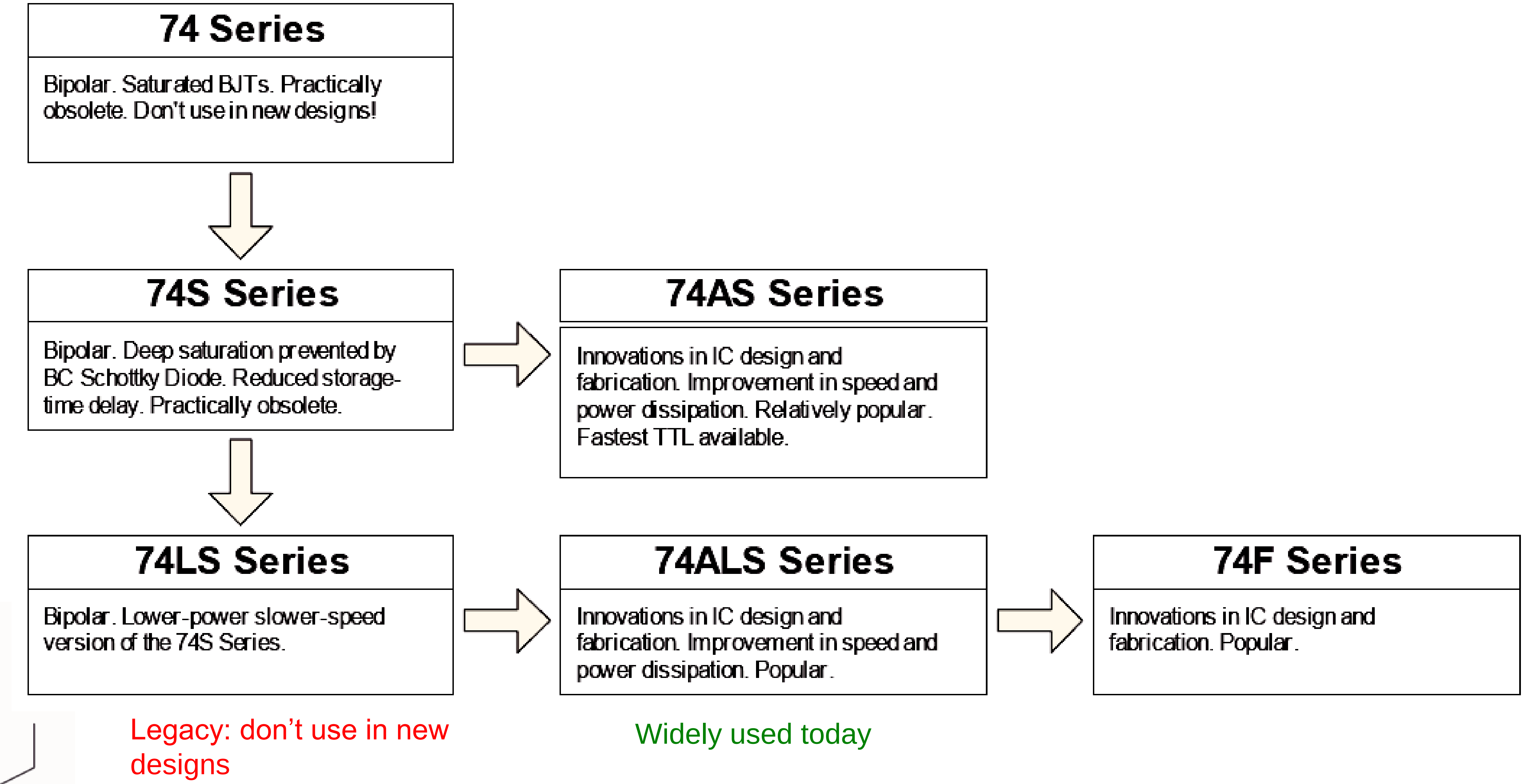
Distinct features

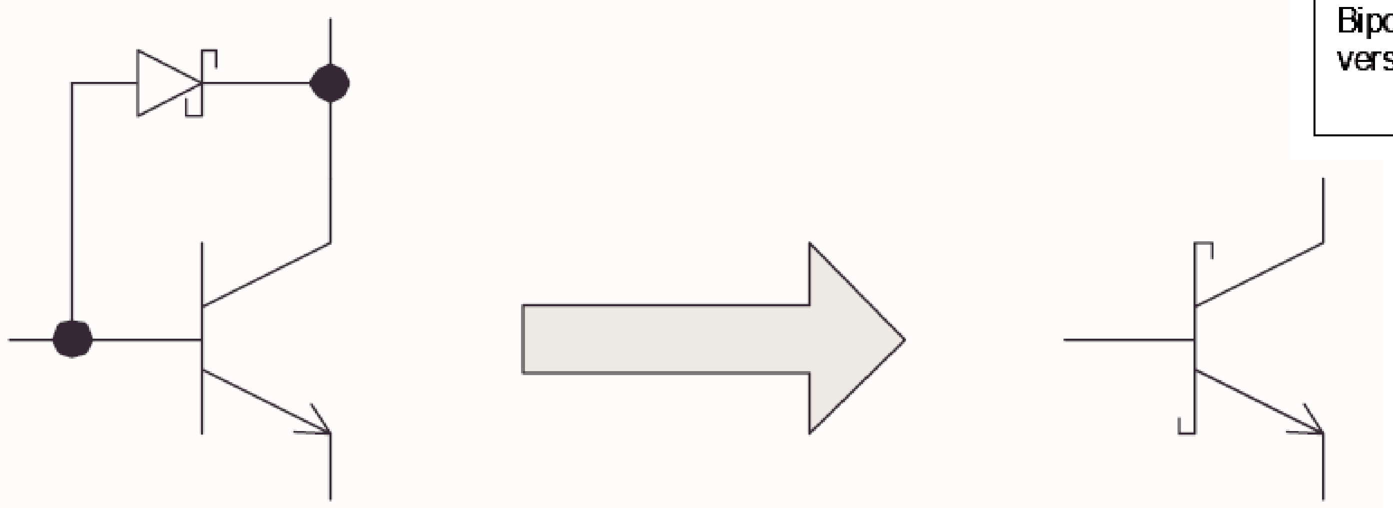
- Multi-emitter transistors
- Totem-pole transistor arrangement

TTL evolution

Schottky series (74LS00) TTL

- A major slowdown factor in BJTs is due to transistors going in/out of saturation
- Shottky diode has a lower forward bias (0.25V)
- When BC junction would become forward biased, the Schottky diode bypasses the current preventing the





ECL

Emitter-Coupled Logic (ECL)

• <u>PROS</u>: Fastest logic family available (~1ns)

• <u>CONS</u>: low noise margin and high power dissipation

• Operated in emitter coupled geometry (recall differential amplifier or emitter-follower), transistors are biased and operate near their Q-point (never near saturation!)

• Logic levels. "0": –1.7V. "1": –0.8V

• Such strange logic levels require extra effort when interfacing to TTL/CMOS logic families.

• Open LTspice example: ECL inverter…

CMOS

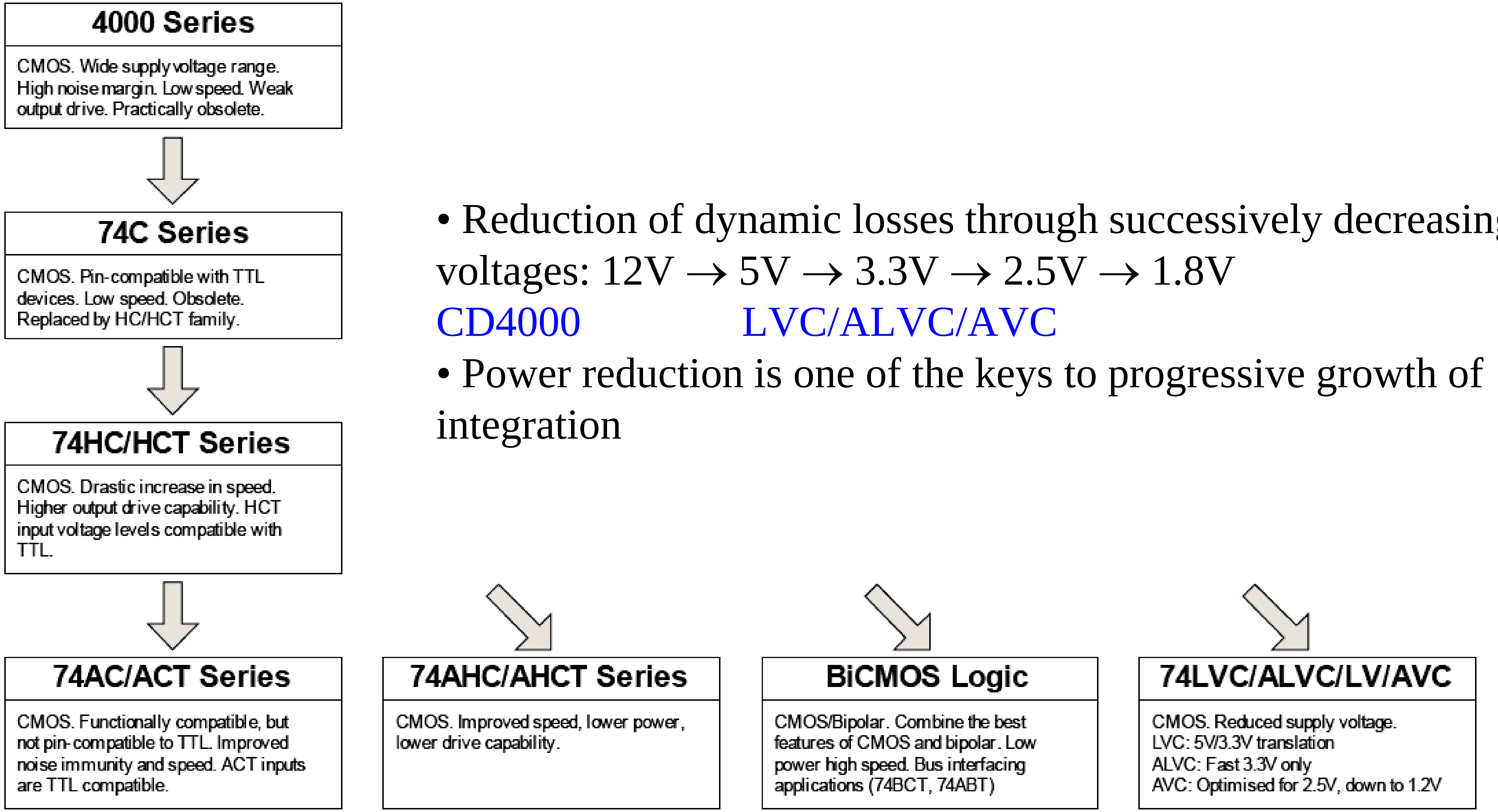
Complimentary MOS (CMOS)

• Other variants: NMOS, PMOS (obsolete)
• Very low static power consumption
• Scaling capabilities (large integration all MOS)
• Full swing: rail-to-rail output
• Things to watch out for:
– don't leave inputs floating (in TTL these will float to HI, in CMOS you get undefined behaviour)
– susceptible to electrostatic damage (finger of death)
• Open LTspice example: CMOS NOT and NAND…

• TTL power essentially constant (no frequency dependence)
• CMOS power scales as $\propto f \times C \times V^2$

• At high frequencies (>> MHz) CMOS dissipates more power than TTL
• Overall advantage is still for CMOS even for very fast chips – only a relatively small portion of complicated circuitry operates at highest frequencies

CMOS



- Reduction of dynamic losses through successively decreasing supply voltages: 12V → 5V → 3.3V → 2.5V → 1.8V

CD4000 LVC/ALVC/AVC

- Power reduction is one of the keys to progressive growth of integration

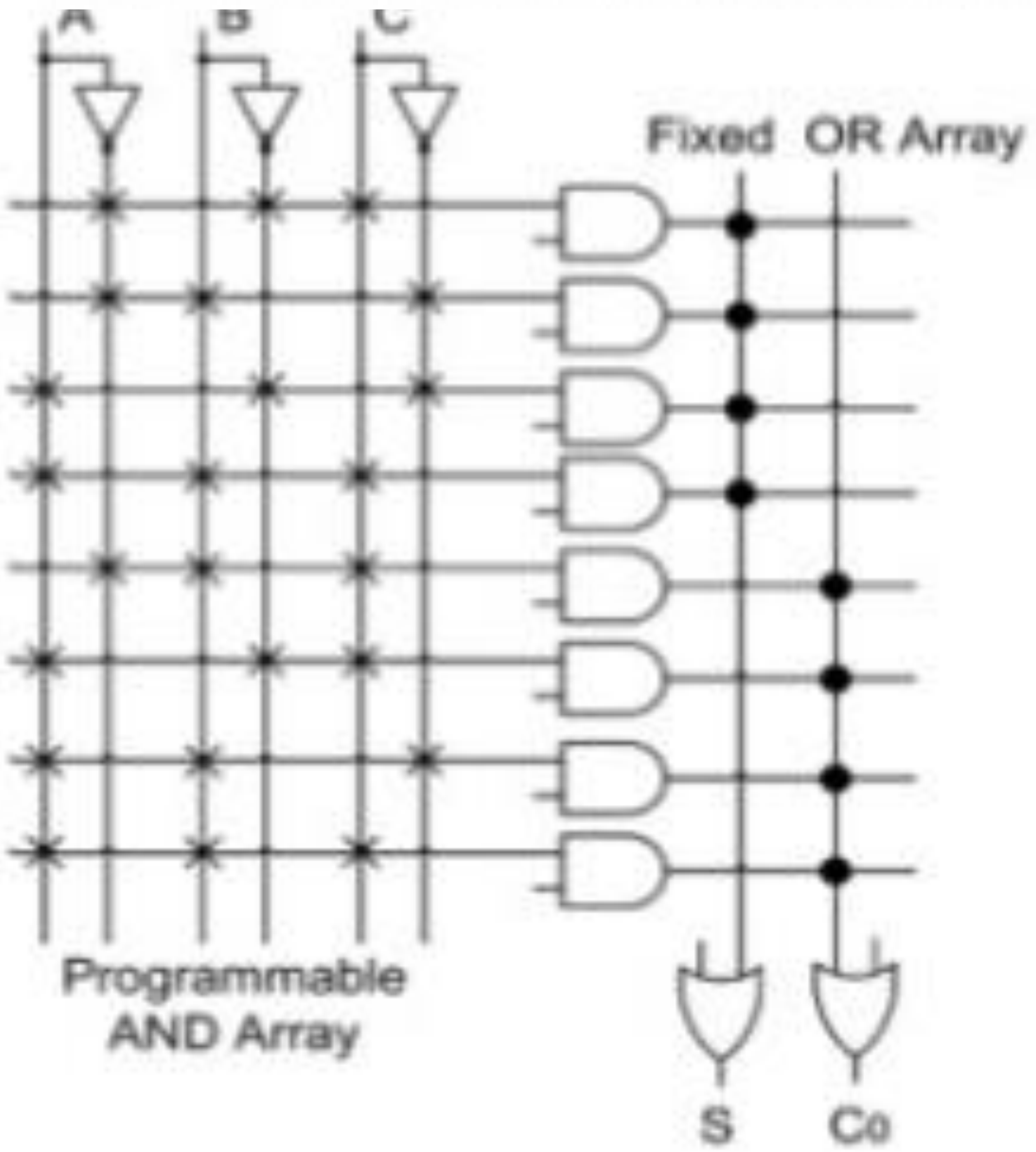
TTL Vs ECL Vs CMOS

	TTL	ECL	CMOS
Base Gate	NAND	OR/NOR	NAND/NOR
Fan-in	12-14	>10	>10
Fan-out	10	25	50
Power dissipation (mW)	10	175	0.001
Noise Margin	0.5V	0.16V (lowest)	1.5V (Highest)
Propagation Delay (ns)	10	<3 lowest	15 Highest
Noise immunity	Very good	good	excellent

Implementation of combinational logic using PROM , PLA and PAL

[ii] PAL has a programmable AND array and a fixed OR array. The full-adder implementation using PAL is shown below:

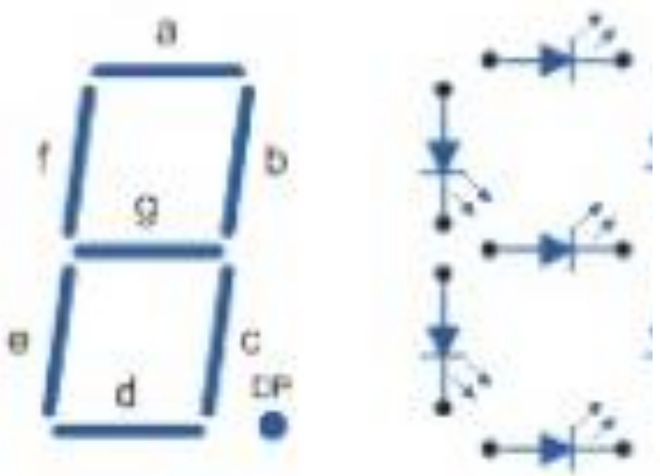
Here, cross mark (X) indicates fusible (programmable) links and dot indicates fixed connections.



Implementation of combinational logic using PROM , PLA and PAL

Problem Give the implementation of BCD-to-7 segment decoder using PLA. Assume common cathode display.

BCD Input				Outputs						
A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	0	0	1	1



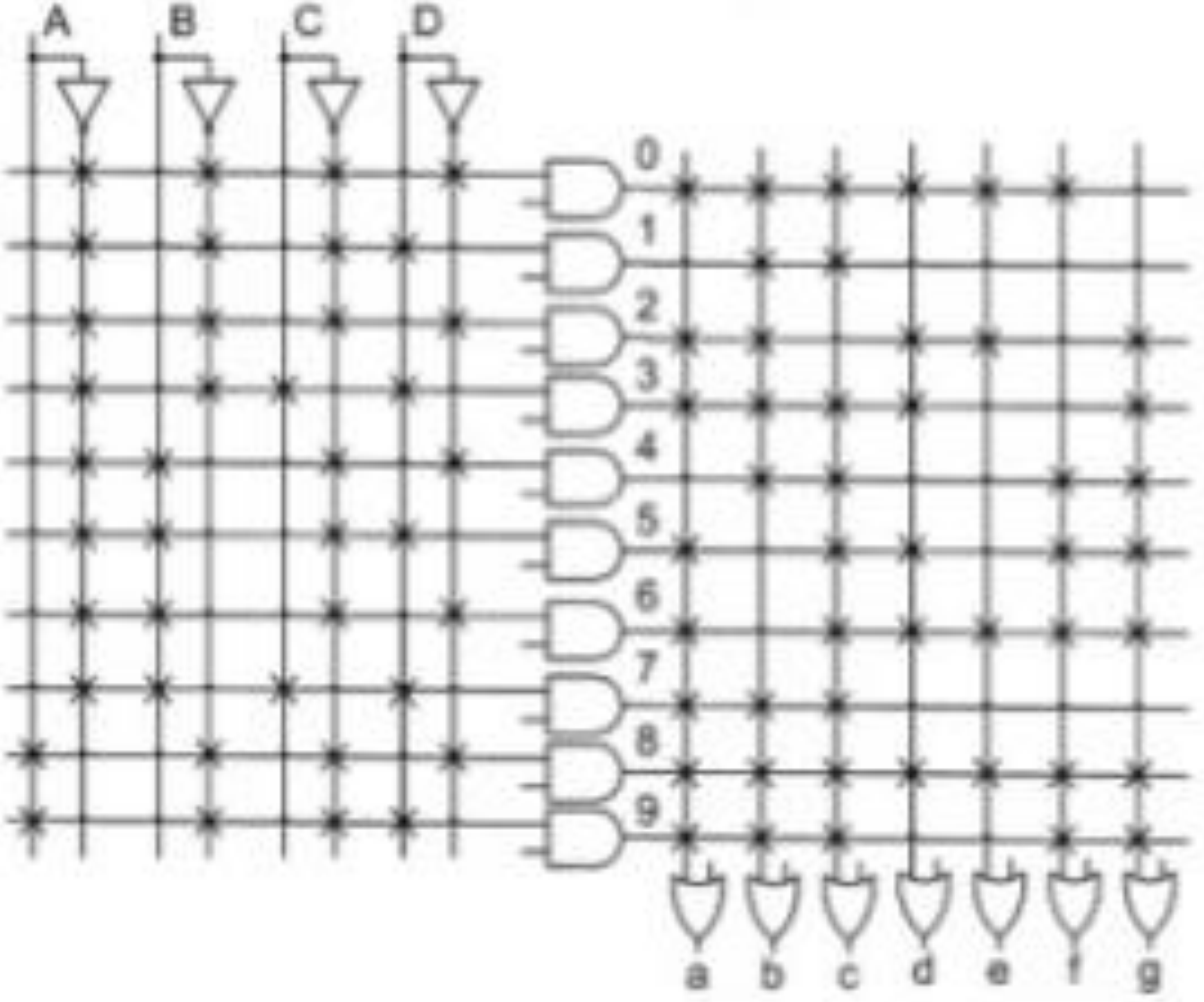
7-Segment display format

Consider the expression for different outputs a, b, c, d, e, f, g

$$a = \sum 0, 2, 3, 5, 6, 7, 8, 9$$
$$b = \sum 0, 1, 2, 3, 4, 7, 8, 9$$
$$c = \sum 0, 1, 3, 4, 5, 6, 7, 8, 9$$
$$d = \sum 0, 2, 3, 5, 6, 8$$
$$e = \sum 0, 2, 6, 8$$
$$f = \sum 0, 4, 5, 6, 8, 9$$

Implementation of combinational logic using PROM , PLA and PAL

The implementation of BCD-to-7 segment decoder using PLA is shown below:



ASSESSMENT - 1

Mux relates with us….

Question 1

Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?

- a) Data Selector
- b) Data distributor
- c) Both data selector and data distributor
- d) DeMultiplexer

Question 2

Which is the major functioning responsibility of the multiplexing combinational circuit?

- a) Decoding the binary information
- b) Generation of all minterms in an output function with OR-gate
- c) Generation of selected path between multiple sources and a single destination
- d) Encoding of binary information

References

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