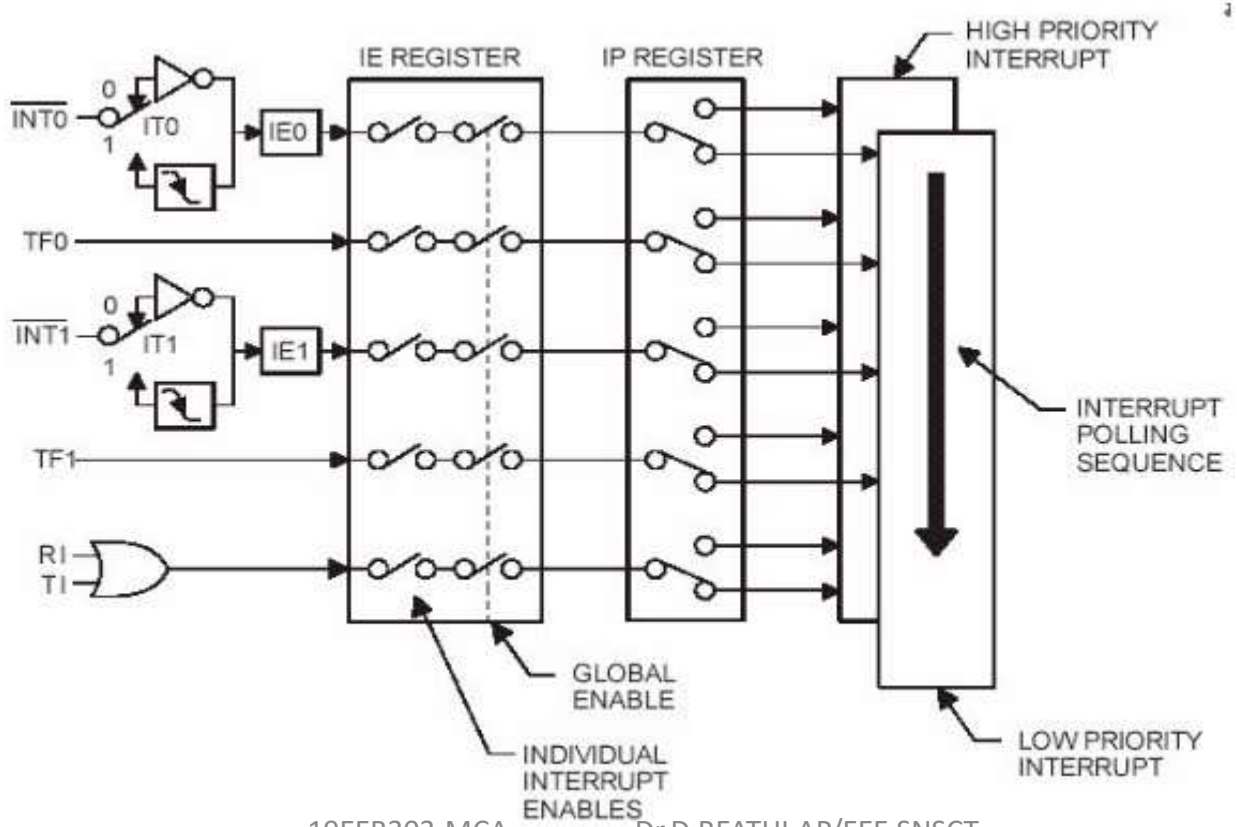
8051 INTERRUPT STRUCTURE

- After 'RESET' all the interrupts get disabled, and therefore, all the interrupts is enabled by software.
- From all the five interrupts, if anyone or all interrupt are activated, this will sets the corresponding interrupt flags.



INTERRUPT ENABLE (IE) REGISTER

- used for enabling and disabling the interrupt.
- This is a bit addressable register in which EA value must be set to one for enabling interrupts.
- The individual bits in this register enables the particular interrupt like timer, serial and external inputs.

EA	--	--	ES	ET1	EX1	ET0	EX0

EA	IE.7	Disables all interrupts, If EA=0, no interrupt will be acknowledged. If EA=1, interrupt source is individually enable or disabled by setting or clearing its enable bit.
--	IE.6	Not implemented, reserved for future use*.
--	IE.5	Not implemented, reserved for future use*.
ES	IE.4	Enable or disable the Serial port interrupt.
ET1	IE.3	Enable or disable the Timer 1 overflow interrupt.
EX1	IE.2	Enable or disable External interrupt 1.
ET0	IE.1	Enable or disable the Timer 0 overflow interrupt.
EX0	IE.0	Enable or disable External interrupt 0.

INTERRUPT PRIORITY (IP) REGISTER

- possible to change the priority levels of an interrupts by clearing or setting the individual bit in (IP) register.
- allows the low priority interrupt can interrupt the high-priority interrupt, but it prohibits the interruption by using another low-priority interrupt.
- If the priorities of interrupt are not programmed, then microcontroller executes the instruction in a predefined manner and its order are INT0, TF0, INT1, TF1, and SI.