SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)

COIMBATORE-35

Accredited by NBA-AICTE and Accredited by NAAC – UGC with A+ Grade

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

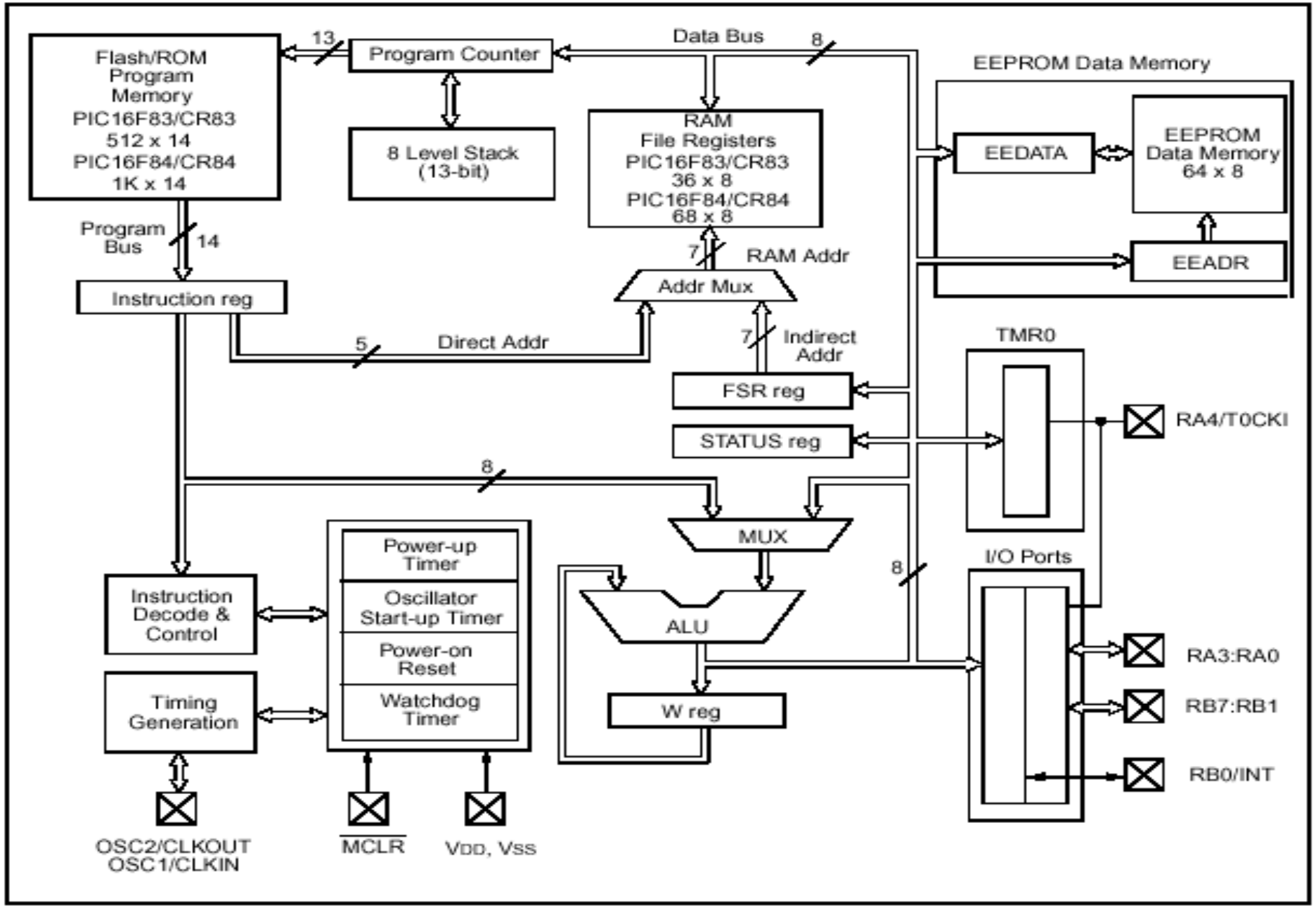
DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

COURSE NAME: 19EEB303 - MICROCONTROLLER AND ITS APPLICATIONS

III YEAR / VI SEMESTER

Unit 2 – PIC MICROCONTROLLER

FIGURE 3-1: PIC16F8X BLOCK DIAGRAM



- The term **PIC** stands for
- "**P**eripheral **I**nterface **C**ontroller"

Salient features

- **Speed :** PIC executes most of its instructions in **0.2 µs** or **five instructions per microsecond**.
- **Instruction set Simplicity :** just **35 instructions.**
- **Integration of operational features:**

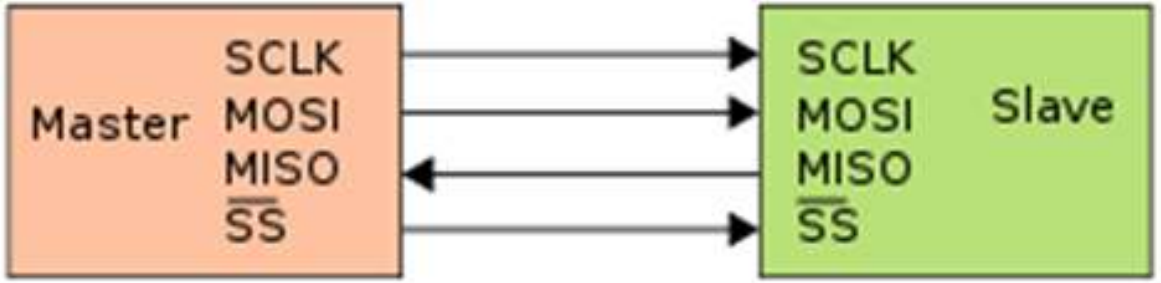
  Power-on-reset and **brown-out protection** ensure that the chip operates only when the supply voltage is within specifications.
- **Watch dog timer:** resets the PIC if the chip malfunctions or deviates from its normal operation at any time.
- **Powerful output pin control:**

  single instruction can **select and drive** a **single output pin high or low in its 0.2 µs** instruction execution time. The PIN can drive a **load of up** to **25µA**.

Features

- **I/O port expansion:**

  With the help of built in **Serial Peripheral Interface (SPI)** the number of I/O ports can be expanded. EPROM/DIP/ROM options are provided.



- **Interrupt control:**

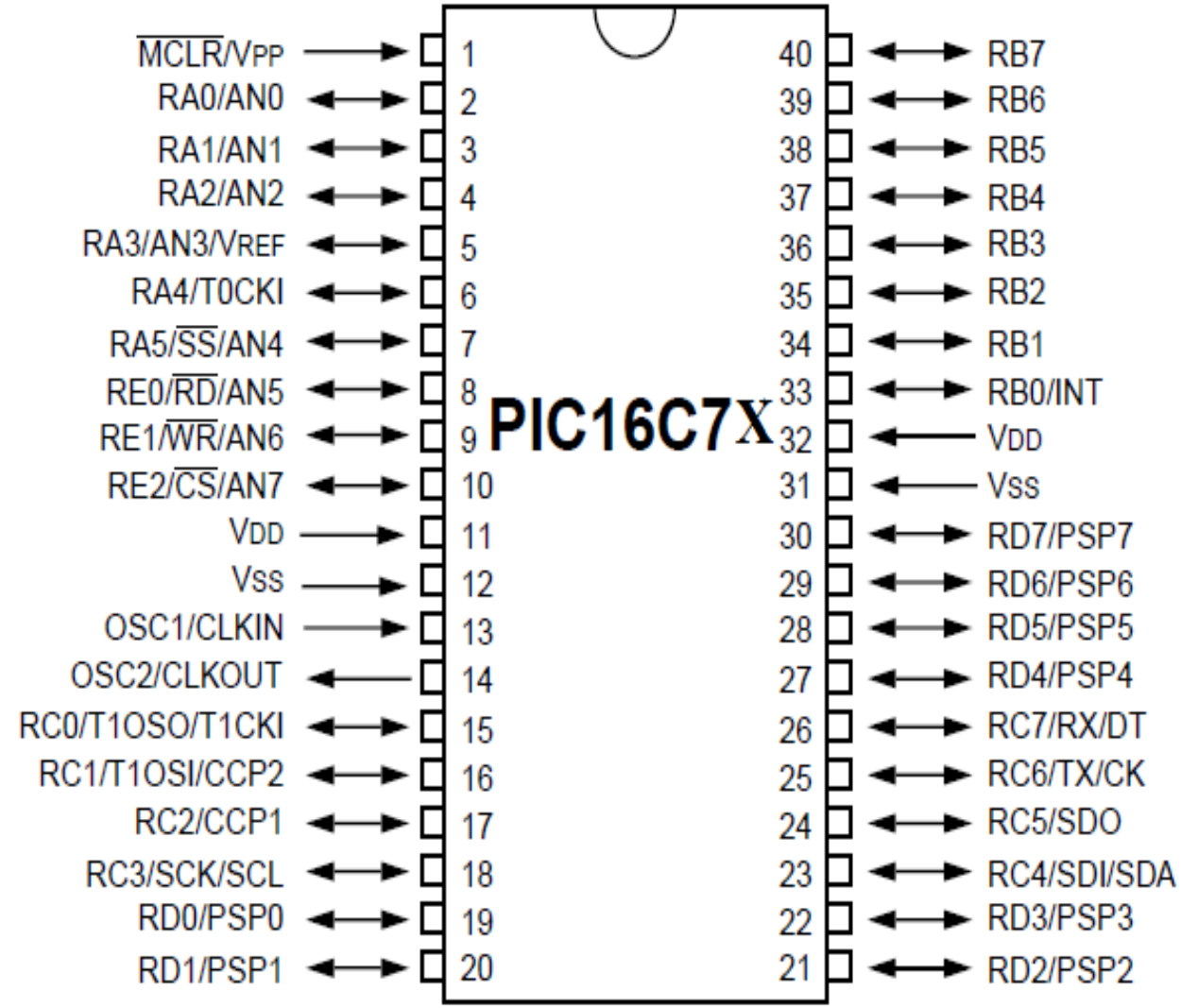
  Up to **12 independent interrupt sources** can control when the CPU will deal with each sources.

- **Programmable timer options:**
- Three timers can characterize inputs, control outputs and provide **internal timing for the program execution**.
- There are Three Timers : Namely **Timer 0**, **Timer1**, **Timer 2**

- **Timer0**: **8-bit timer/counter** with **8-bit prescaler**

- **Timer1**:**16-bit timer/counter** with **prescaler can be incremented during sleep via external crystal/clock**

- **Timer2**: **8-bit timer/counter** with **8-bit period register, pre- scaler and post- scaler**


MCLR/VPP 1
RA0/AN0 2
RA1/AN1 3
RA2/AN2 4
RA3/AN3/VREF 5
RA4/T0CKI 6
RA5/SS/AN4 7
RE0/RD/AN5 8
RE1/WR/AN6 9
RE2/CS/AN7 10
VDD 11
VSS 12
OSC1/CLKIN 13
OSC2/CLKOUT 14
RC0/T1OSO/T1CKI 15
RC1/T1OSI/CCP2 16
RC2/CCP1 17
RC3/SCK/SCL 18
RD0/PSP0 19
RD1/PSP1 20
PIC16C7X
40 RB7
39 RB6
38 RB5
37 RB4
36 RB3
35 RB2
34 RB1
33 RB0/INT
32 VDD
31 VSS
30 RD7/PSP7
29 RD6/PSP6
28 RD5/PSP5
27 RD4/PSP4
26 RC7/RX/DT
25 RC6/TX/CK
24 RC5/SDO
23 RC4/SDI/SDA
22 RD3/PSP3
21 RD2/PSP2

CENTRAL PROCESSOR UNIT (CPU):

- CPU is manufactured in **RISC.**
- RISC stands for **Reduced Instruction Set Computer.**
- Capable of recognizing and executing only **35 simple instructions.**
- Execution time instructions = **4 clock cycles.**
- Execution time of each instruction = **200nS**
- Jump and branch instructions the execution time = **2 clock cycles.**

- Operating frequency = **20MH.**
- Execute **5 million instructions / second**

CPU REGISTERS

The CPU registers are

- **Working Register (W)**
- **Status – Register**
- **FSR – File Select Register**
- **INDF**
- **PCLATH**
- **Program Counter**
- **PCL**
- **Eight Level Stack**
- **All SFR in PIC are ___8___ bits size**

Working Register:(W)

Temporary holding register.

Called as **Accumulator.**

Cannot be access **Directly**

W content moved to some other register and then it can be accessed.

used by many instructions as **source of an operand**.

destination for the result of instruction execution.

It is a **8-bit** regarding.

Status Register: can be **destination** for any instruction

contains : **arithmetic status** of the ALU

reset Status, bank select bits for data memory.

FSR – (File Select Register): Special Purpose Register

- **Indirect addressing.**
- **8-bit register file - address pointer**
- any address is **first written** in FSR access **entire register file**.

INDF – (Indirect File): Special Purpose Register

- Is not a Physical Register
- Addressing INDF - Addresses Register address in FSR

Program Counter: (PC)

13 bit wide

PCL 8 Bit – Readable

PCH 5 Bit – Not Readable