SNS COLLEGE OF TECHNOLOGY

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COIMBATORE-35
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19EET103 / ELECTRIC CIRCUITS AND ELECTRON DEVICES

UNIT 4- ELECTRONIC DEVICES AND APPLICATIONS

JFET

OUTLINE

- Field Effect Transistor (FET)
- Junction Field Effect Transistor (JFET)
- Construction of JFET
- Theory of Operation
- I-V Characteristic Curve
- Pinch off Voltage (V_P)
- Saturation Level
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- Cut off Voltage
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INTRODUCTION

The ordinary or bipolar transistor has two main disadvantage.

- It has a low input impedance
- It has considerable noise level

To overcome this problem Field effect transistor (FET) is introduced because of its:

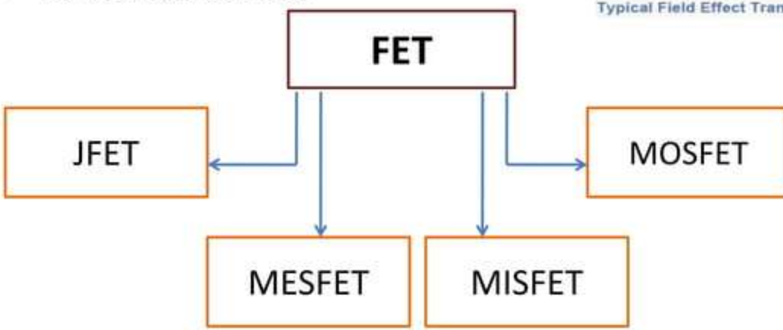
- High input impedance
- Low noise level than ordinary transistor

And Junction Field Effect Transistor (JFET) is a type of FET.

Field Effect Transistor (FET)

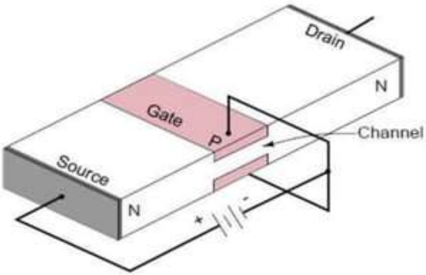
- FET is a voltage controled device.
- It consists of three terminal .
  - Gate
  - Source
  - Drain
- It is classified as four types.

Typical Field Effect Transistor



Junction Field Effect Transistor (JFET)

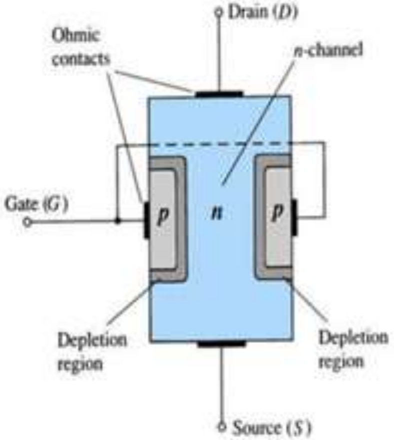
❑ **Junction Field Effect Transistor** is a three terminal semiconductor device in which current conducted by one type of carrier i.e. by electron or hole.



Junction field effect transistor

Construction of JFET

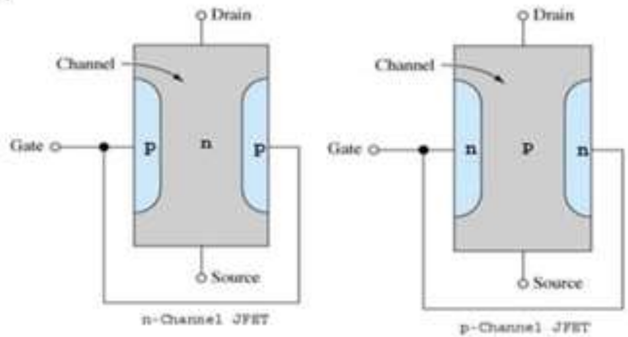
- **Source:** The terminal through which the majority carriers enter into the channel, is called the *source* terminal S .
- **Drain:** The terminal, through which the majority carriers leave from the channel, is called the *drain* terminal D .
- **Gate:** There are two internally connected heavily doped impurity regions to create two P-N junctions. These impurity regions are called the *gate* terminal G.
- **Channel:** The region between the source and drain, sandwiched between the two gates is called the *channel* .



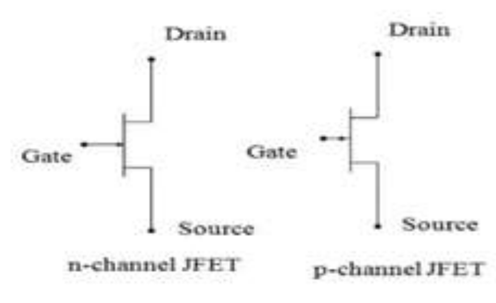
Types of JFET

➢ JFET has two types :

- n- Channel JFET
- p- Channel JFET



Symbol of JFET



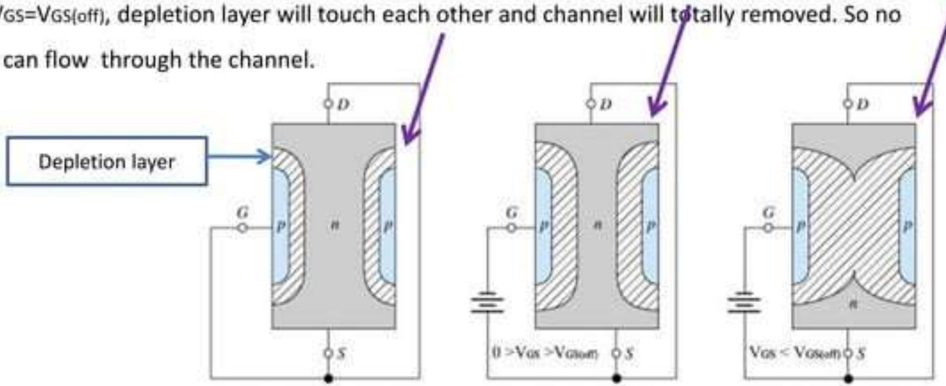
Features of JFET

- JFET is a voltage controlled device i.e. input voltage (V_{GS}) control the output current (I_D).
- In JFETs, the width of a junction is used to control the effective cross-sectional area of the channel through which current conducts.
- It is always operated with Gate-Source p-n junction in reverse bias.
- Because of reverse bias it has high input impedance.
- In JFET the gate current is zero i.e. I_G=0.

Theory of Operation

(i) When gate-source voltage(V_{GS}) is applied and drain-source voltage is zero i.e. V_{DS}= 0V

- When V_{GS} = 0v , two depletion layers & channel are formed normally.
- When V_{GS} increase negatively i.e. 0V > V_{GS} > $V_{GS(off)}$, depletion layers are also increased and channel will be decrease.
- When V_{GS}=$V_{GS(off)}$, depletion layer will touch each other and channel will totally removed. So no current can flow through the channel.



(a) Bias is zero and depletion layer is thin hence channel resistance is low.

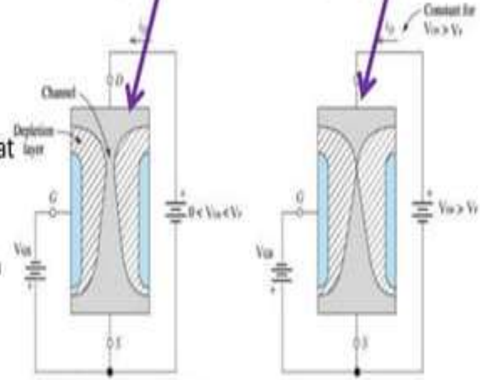
(b) V_{GS} is applied hence depletion layer is increased. So less charge can be flow through the channel.

(c) V_{GS} is geater than cut off voltage hence no coductive path exist.

Theory of Operation

(ii) When drain-source voltage (V_{DS}) is applied at constant gate-source voltage (V_{GS}) :

- Now reverse bias at the drain end is larger than source end and so the depletion layer is wider at the drain end than source end.
- When V_{DS} increases i.e. $0v < V_{DS} < V_P$, depletion layer at drain end is gradually increased and drain current also increased.
- When $V_{DS} = V_P$ the channel is effectively closed at drain end and it does not allow further increase of drain current. So the drain current will become constant.



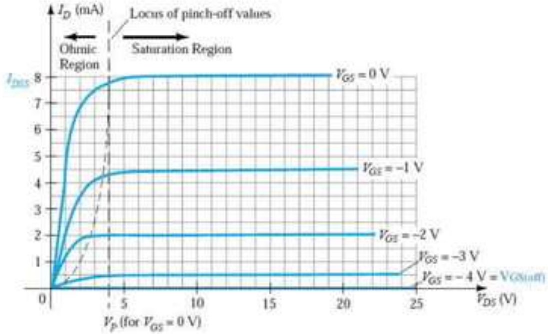
(a) Channel becomes narrower as V_{DS} is increased

(b) Current is confined to a very narrow strip for $V_{DS} > V_P$

I-V Characteristic Curve

It is the curve between drain current (I_D)and drain-source voltage (V_{DS})for different gate-source voltage (V_{GS}). It can be characterized as:

- For V_{GS}=0v the drain current is maximum. It's denoted as I_{DSS} and called shorted gate drain current.
- Then if V_{GS} increases Drain current I_D decreases ($I_D < I_{DSS}$) even though V_{DS} is increased.
- When V_{GS} reaches a certain value, the drain current will be decreased to zero.
- For different V_{GS}, the I_D will become constant after pinch off voltage (V_P) though V_{DS} is increased.



Transfer Characteristic Curve

- This curve shows the value of I_D for a given value of V_{GS} .

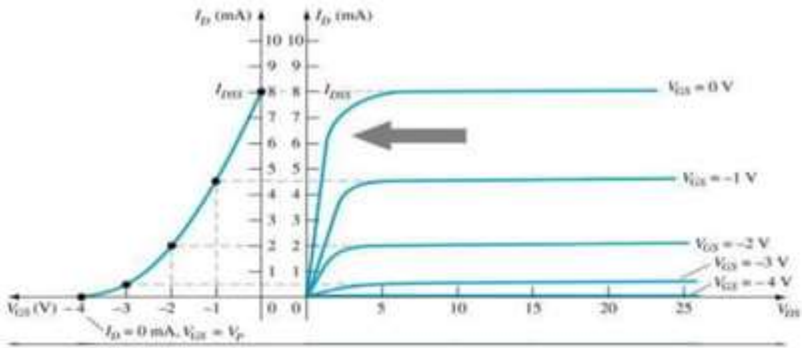
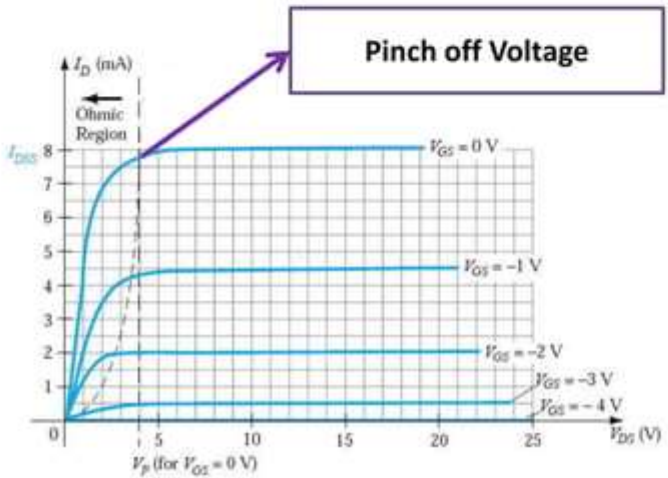


Fig: Transfer Characteristic Curve

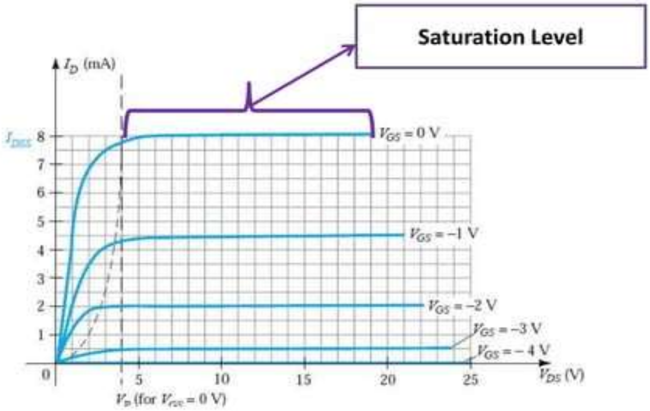
Pinch off Voltage (V_P)

- It is the minimum drain source voltage at which the drain current essentially become constant.



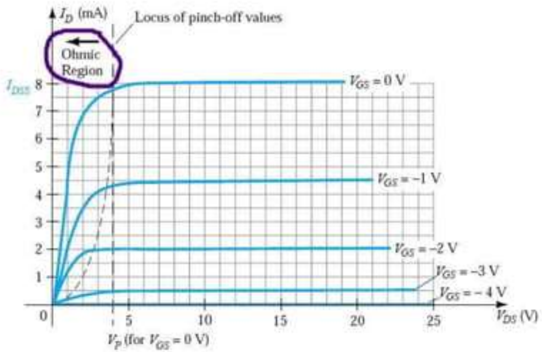
Saturation Level

- After pinch off voltage the drain current become constant, this constant level is known as saturation level .



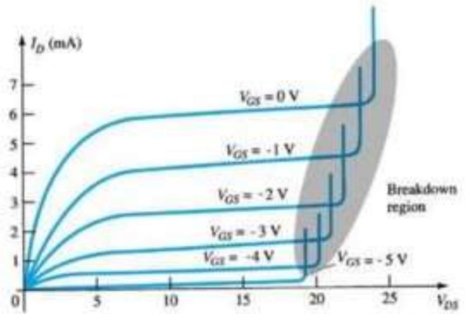
Ohmic Region

- The region behind the pinch off voltage where the drain current increase rapidly is known as Ohmic Region.



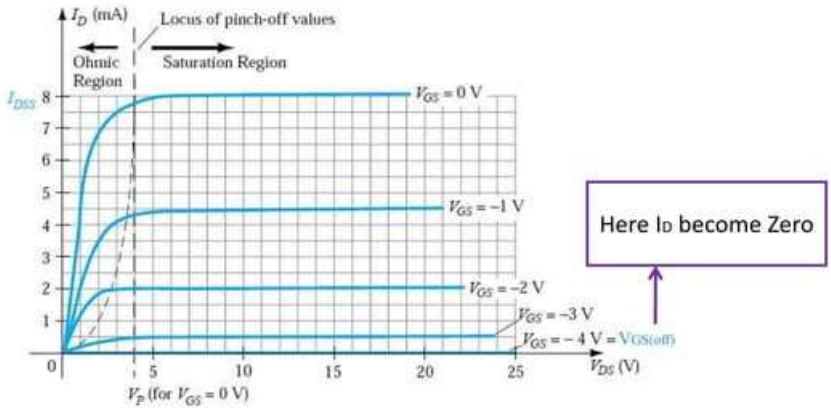
Break Down Region

- It is the region, when the drain-source voltage (V_{DS}) is high enough to cause the JFET's resistive channel to breakdown and pass uncontrolled maximum current .



Cut off Voltage

- The gate-source voltage, when the drain current become zero is called cut-off voltage. Which is usually denoted as $V_{GS}(off)$.



Advantages

- It is simpler to fabricate, smaller in size.
- It has longer life and higher efficiency.
- It has high input impedance.
- It has negative temperature coefficient of resistance .
- It has high power gain.

Disadvantages

- Greater susceptibility to damage in its handling.
- JFET has low voltage gain.

Application of JFET

- Voltage controlled resistor
- Analog switch or gate
- Act as an amplifier
- Low-noise amplifier
- Constant current source