SNS COLLEGE OF TECHNOLOGY

An Autonomous Institution

Coimbatore-35

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A++' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ITT204 - MICROCONTROLLER AND EMBEDDED SYSTEMS

II YEAR/ IV SEMESTER

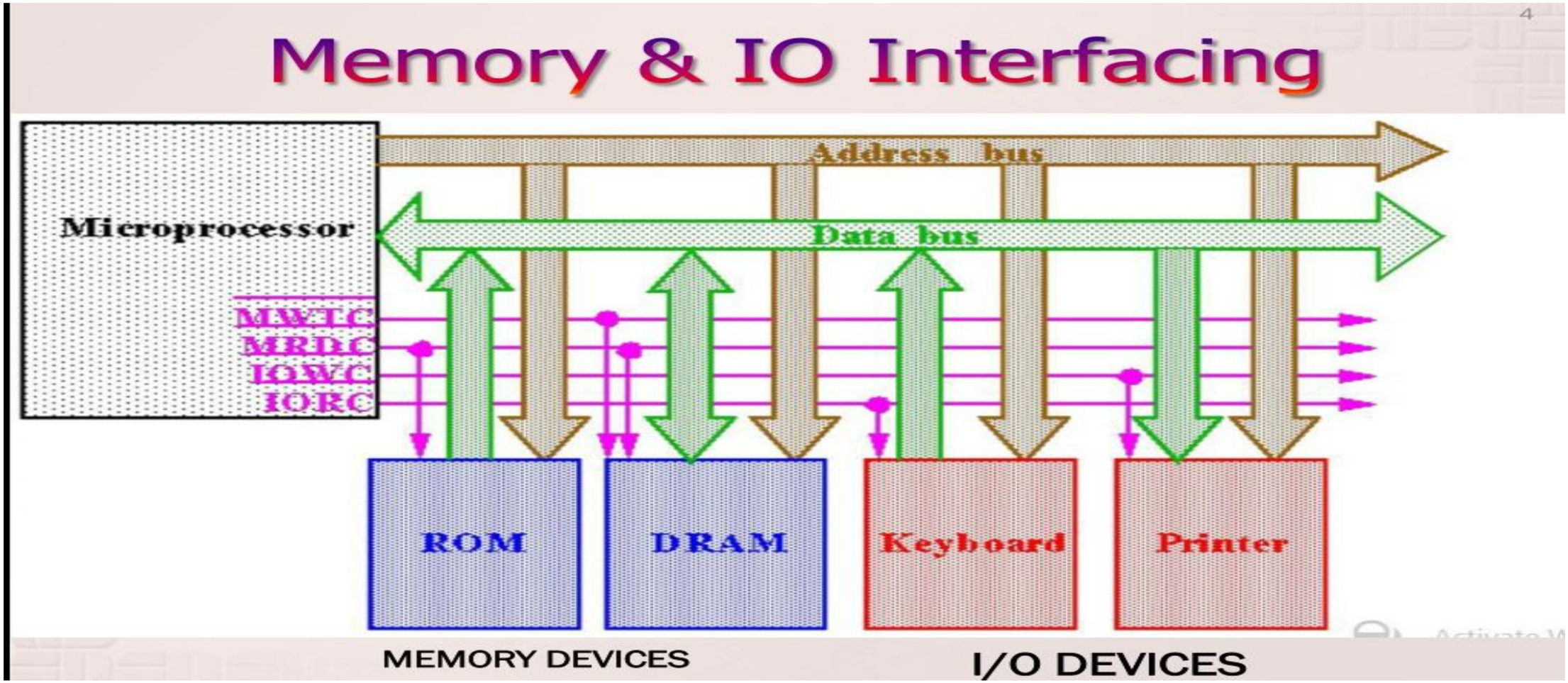
UNIT II PERIPHERAL INTERFACING

TOPIC – Interfacing Requirements - Memory Mapped I/O- I/O Mapped I/O

OUTLINE

Data Transfers

- **Synchronous** ----- Usually occur when peripherals are located within the same computer as the CPU. Close proximity allows all state bits change at same time on a common clock.
- **Asynchronous** ----- Do not require that the source and destination use the same system clock.


Memory & IO Interfacing
Microprocessor
MWTC
MRDC
IOWC
IORC
Address bus
Data bus
ROM
DRAM
Keyboard
Printer
MEMORY DEVICES
I/O DEVICES

- interface memory (RAM, ROM, EPROM'...) or I/O devices to 8086 microprocessor. Several **memory chips** or **I/O devices** can connected to a microprocessor. An address decoding circuit is used to select the required I/O device or a memory chip.

IO mapped IO V/s Memory Mapped IO

Memory Mapped IO

- IO is treated as memory.
- 16-bit addressing.
- More Decoder Hardware.
- Can address 2^{16}=64k locations.
- Less memory is available.

IO Mapped IO

- IO is treated IO.
- 8- bit addressing.
- Less Decoder Hardware.
- Can address 2^{8}=256 locations.
- Whole memory address space is available.

Memory Mapped IO

- Memory Instructions are used.
- Memory control signals are used.
- Arithmetic and logic operations can be performed on data.
- Data transfer b/w register and IO.

IO Mapped IO

- Special Instructions are used like IN, OUT.
- Special control signals are used.
- Arithmetic and logic operations can not be performed on data.
- Data transfer b/w accumulator and IO.

THANK YOU