



SNS COLLEGE OF TECHNOLOGY

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Coimbatore-35



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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ITT204 - MICROCONTROLLER AND EMBEDDED SYSTEMS

II YEAR/ IV SEMESTER

UNIT II PERIPHERAL INTERFACING

TOPIC – 8255 PPI



Parallel communication interface INTEL 8255



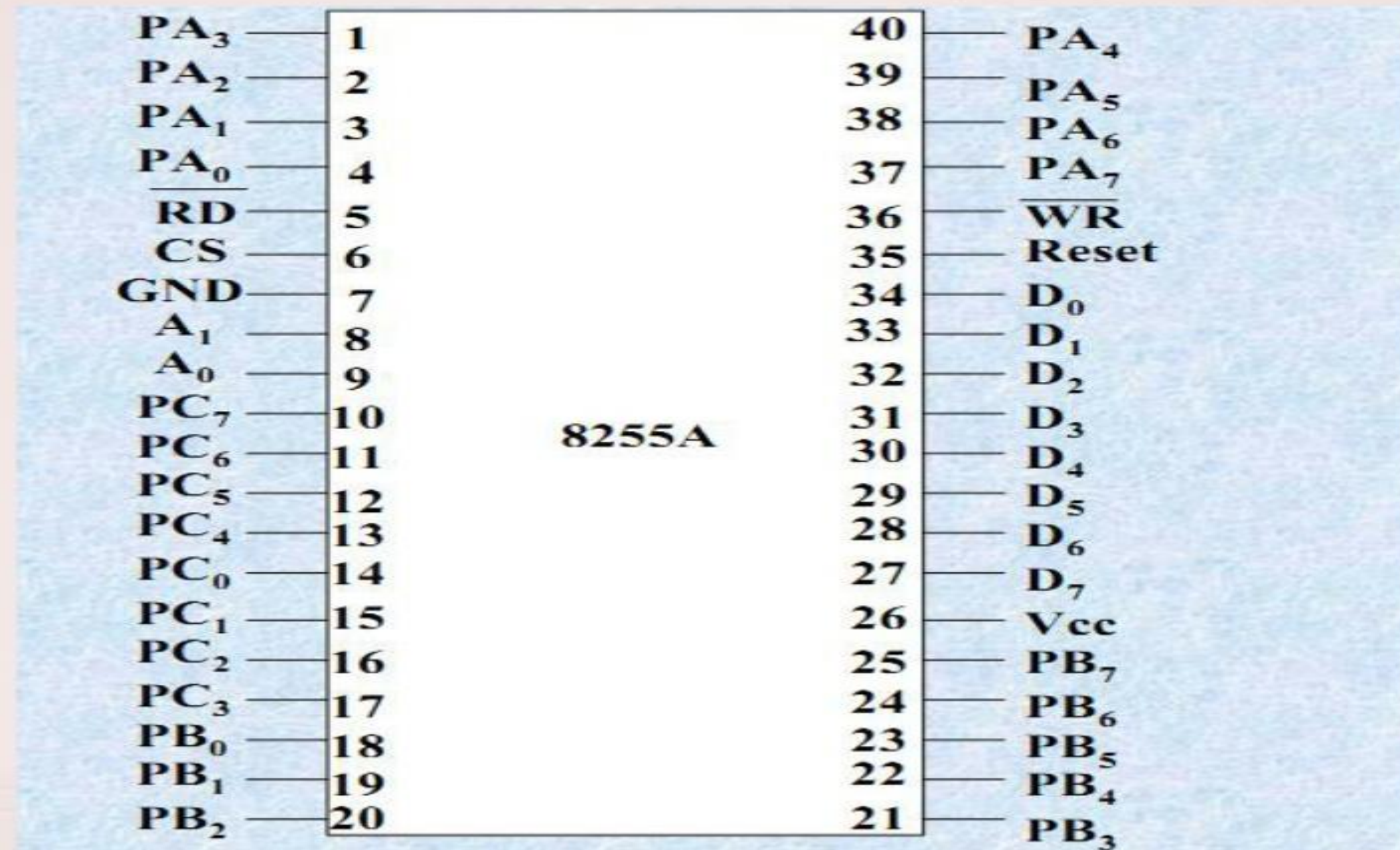


8255 PPI

- The 8255 chip is also called as **Programmable Peripheral Interface**.
- The Intel's 8255 is designed for use with Intel's 8-bit, 16-bit and higher capability microprocessors
- The 8255 is a 40 pin integrated circuit (IC), designed to perform a variety of interface functions in a computer environment.
- It is flexible and economical.

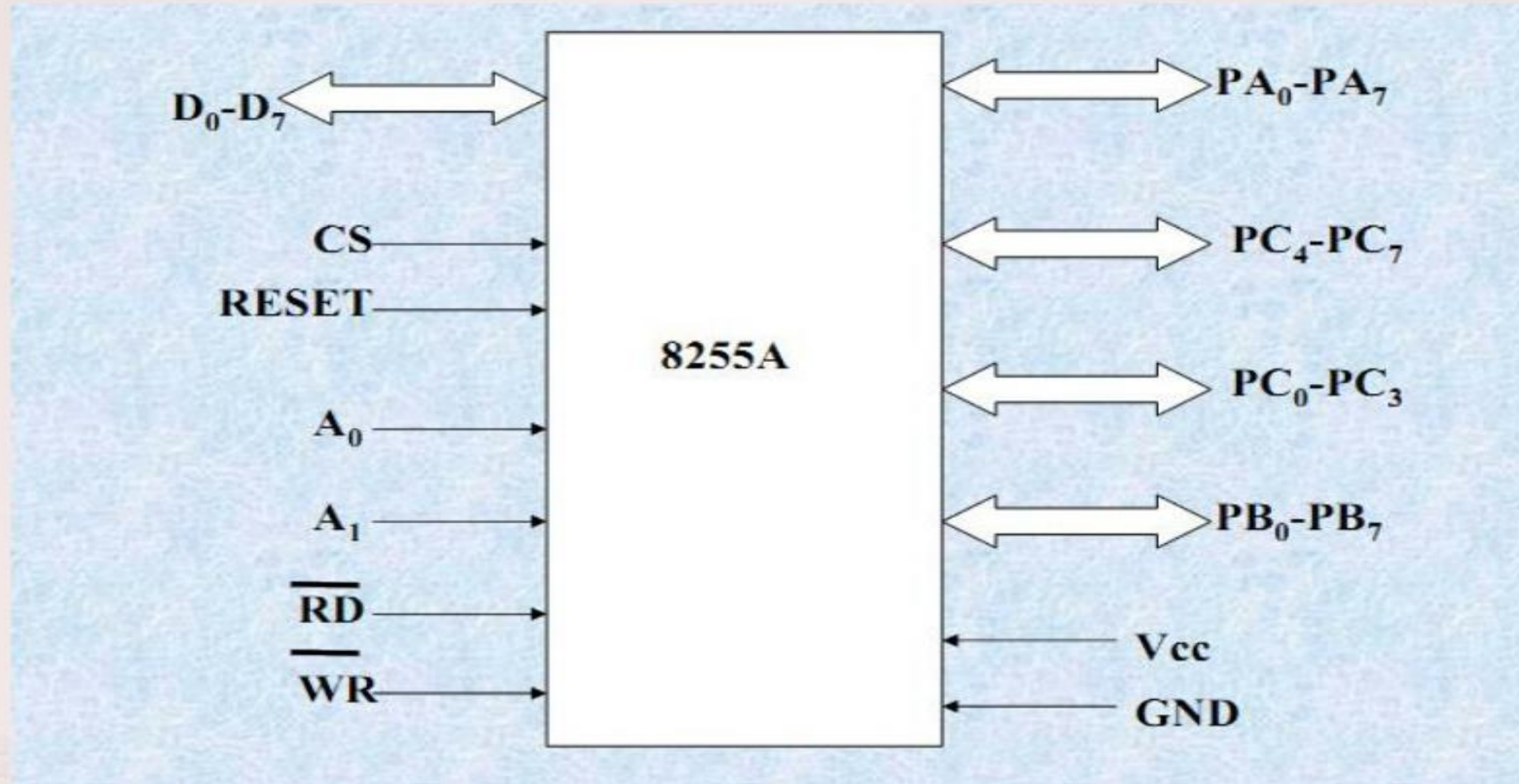


PIN DIAGRAM OF 8255





Signals of 8085





8255 PIO/PPI

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- ❑ It has **24 input/output** lines which may be individually programmed.
- ❑ 2 groups of I/O pins are named as
 - Group A (Port-A & Port C Upper)**
 - Group B (Port-B & Port C Lower)**
- ❑ **3 ports**(each port has 8 bit)
 - Port A** lines are identified by symbols **PA₀-PA₇**
 - Port B** lines are identified by symbols **PB₀-PB₇**
 - Port C** lines are identified by **PC₀-PC₇** , **PC₃-PC₀**
ie: **PORT C UPPER(PC₇-PC₄) , PORT C LOWER(PC₃-PC₀)**



D0 - D7: data input/output lines for the device. All information read from and written to the 8255 occurs via these 8 data lines.

\overline{CS} (Chip Select). If this line is a logical 0, the microprocessor can read and write to the 8255.

RESET : The 8255 is placed into its reset state if this input line is a logical 1



- **\overline{RD}** : This is the input line driven by the microprocessor and should be **low** to indicate **read operation** to 8255.
- **\overline{WR}** : This is an input line driven by the microprocessor. A **low** on this line indicates **write operation**.
- **A1-A0** : These are the address input lines and are driven by the microprocessor.



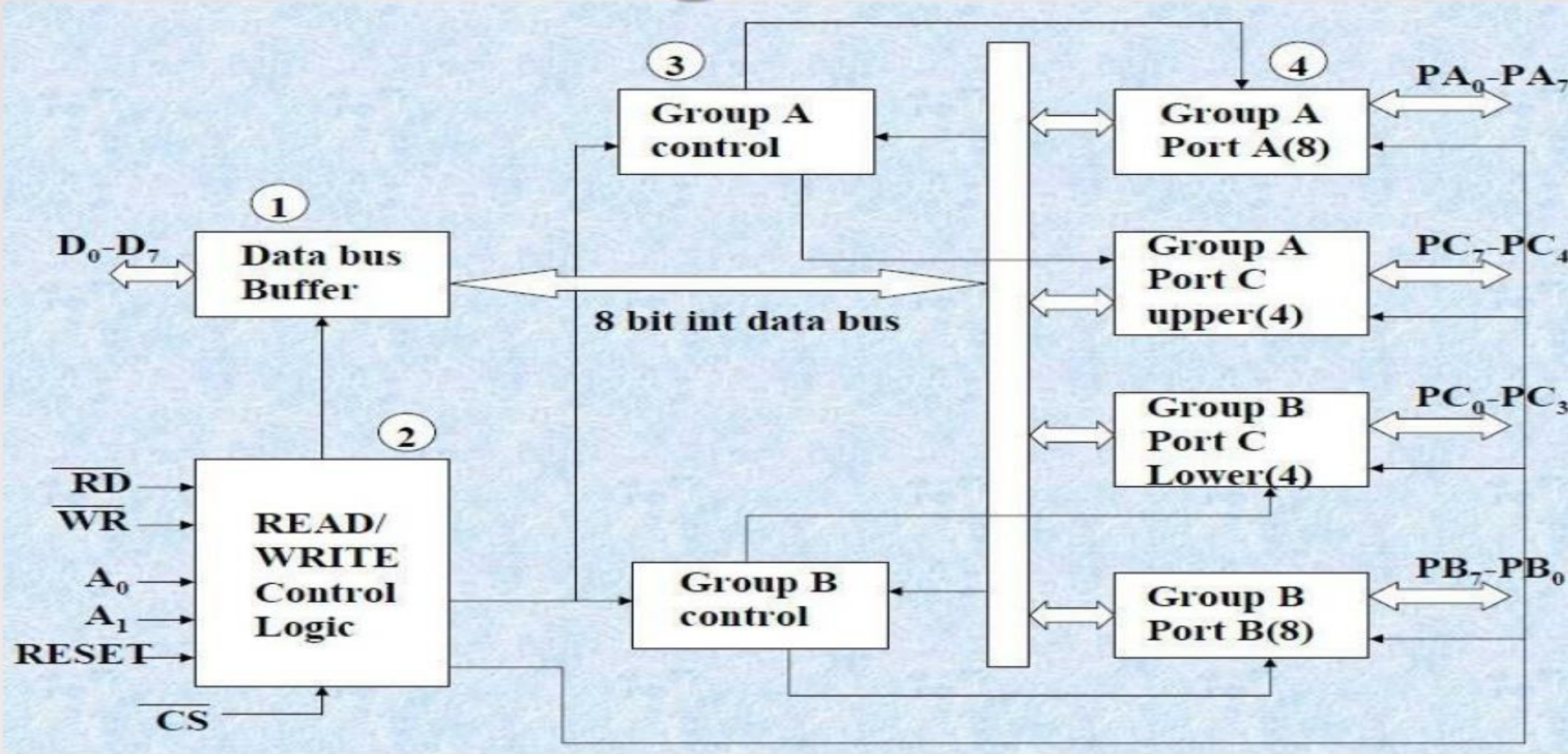
Control Logic

- \overline{CS} signal is the master Chip Select
- A0 and A1 specify one of the two I/O Ports

\overline{CS}	A1	A0	Selected
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control Register
1	X	X	8255 is not selected



Block Diagram of 8255A





Block Diagram of 8255 (Architecture)

It has a 40 pins of 4 parts.

1. Data bus buffer
2. Read/Write control logic
3. Group A and Group B controls
4. Port A, B and C



1. Data bus buffer

- This is a tristate bidirectional buffer used to interface the 8255 to system data bus. Data is transmitted or received by the buffer on execution of input or output instruction by the CPU.



2. Read/Write control logic

- This unit accepts control signals (RD, WR) and also inputs from address bus and issues commands to individual group of control blocks (Group A, Group B).
- It has the following pins.

$\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, RESET , A1 , A0



3. Group A and Group B controls

- These block **receive control** from the **CPU** and **issues commands** to their respective ports.

Group A - PA and PCU (PC7 –PC4)

Group B – PB and PCL (PC3 –PC0)

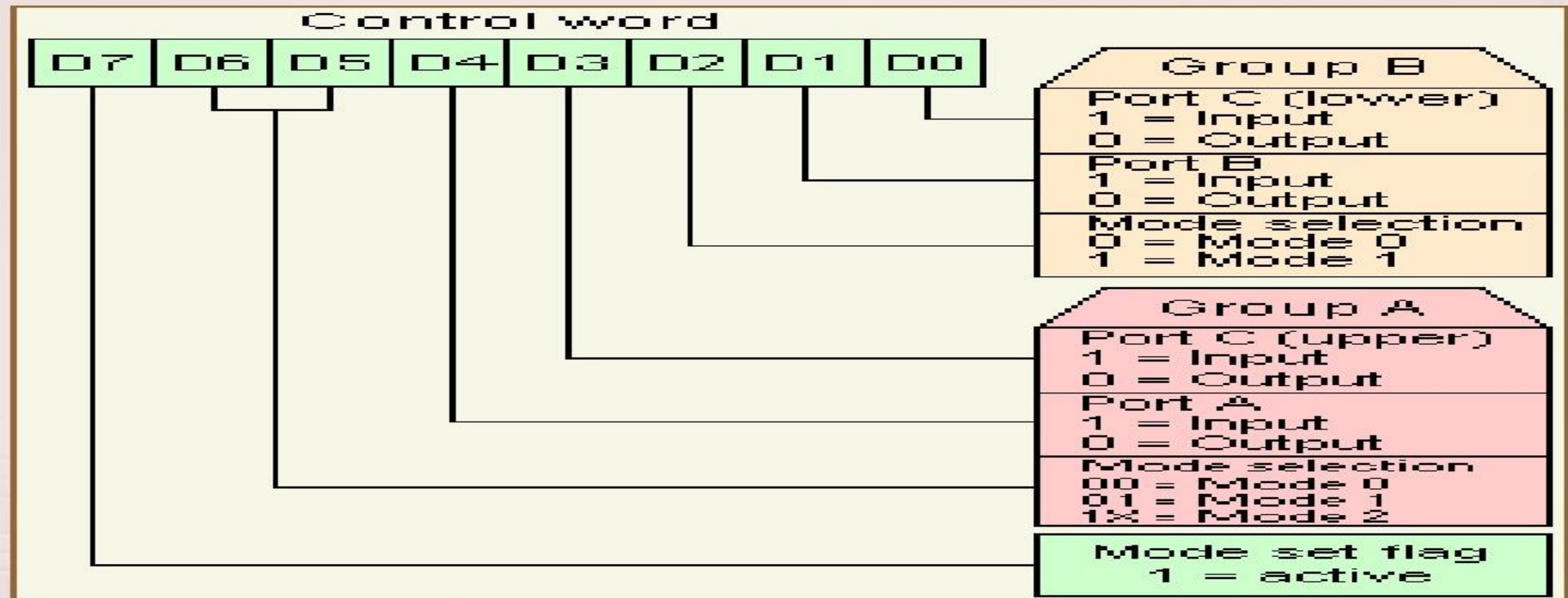
- a) **Port A:** This has an 8 bit latched/buffered O/P and 8 bit input latch. It can be programmed in 3 modes – **mode 0, mode 1, mode 2.**



- b) Port B: It can be programmed in **mode 0, mode1**
- c) Port C : It can be programmed in **mode 0**



CONTROL WORD REGISTER(CWR)





Modes of Operation of 8255

- **Bit Set/Reset(BSR) Mode**
 - ✖ **Set/Reset bits in Port C**
- **I/O Mode**
 - ✖ **Mode 0 (Simple input/output)**
 - ✖ **Mode 1 (Handshake mode)**
 - ✖ **Mode 2 (Bidirectional Data Transfer)**



1. BSR Mode



8255 Control Register format for BSR Mode



B3	B2	B1	Bit/ pin of port C selected
0	0	0	PC₀
0	0	1	PC₁
0	1	0	PC₂
0	1	1	PC₃
1	0	0	PC₄
1	0	1	PC₅
1	1	0	PC₆
1	1	1	PC₇

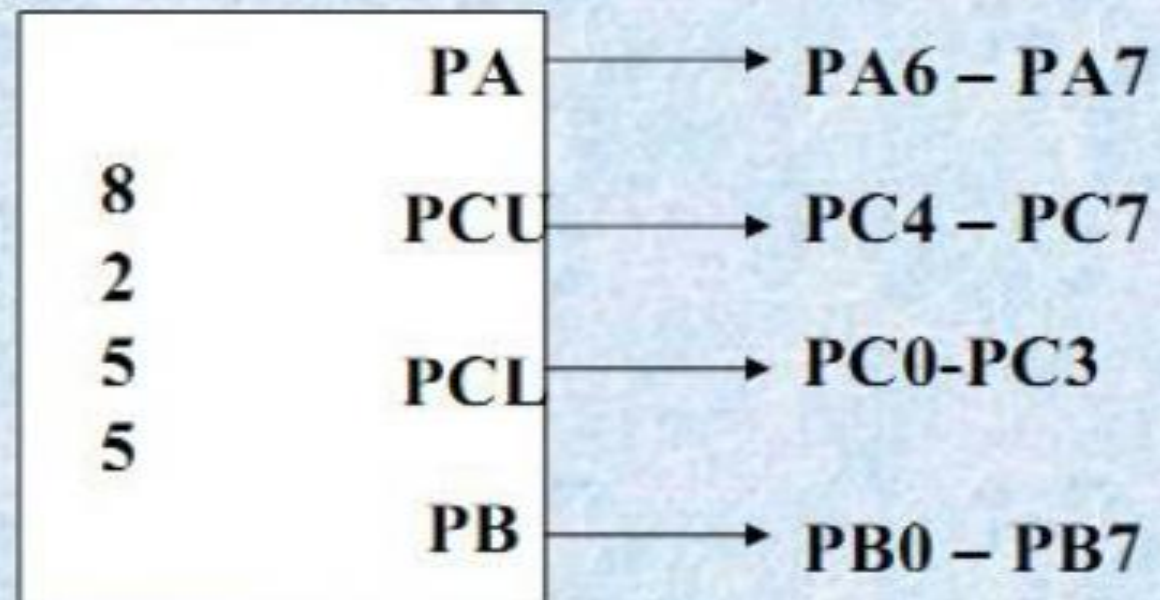
Concerned only with the 8-bits of Port C.
Set or Reset by control word
Ports A and B are not affected



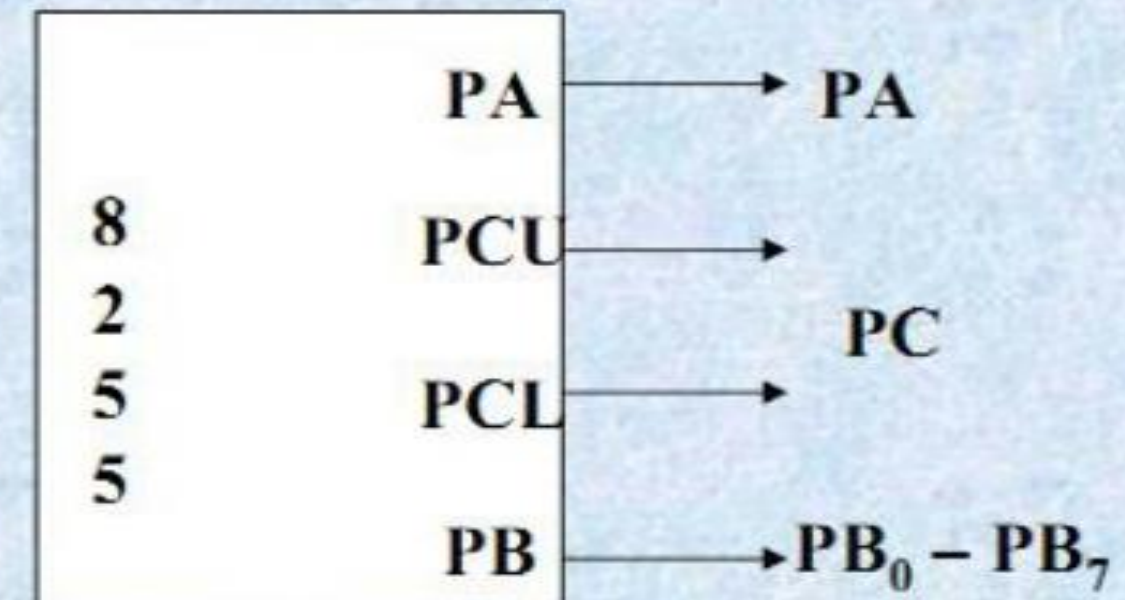
2. I/O MODE

a) Mode 0 (Simple Input or Output):

- Ports A and B are used as Simple I/O Ports
- Port C as two 4-bit ports
- **Features**
 - Outputs are latched
 - Inputs are not latched
 - Ports do not have handshake or interrupt capability



All Output



Port A and Port C acting as O/P. Port B acting as I/P

Mode 0



b) Mode 1: (Input or Output with Handshake)

- Handshake signals are exchanged between MPU & Peripherals
 - **Features**
 - Ports A and B are used as Simple I/O Ports
 - Each port uses 3 lines from Port C as handshake signals
 - Input & Output data are latched
 - interrupt logic supported



c) Mode 2: Bidirectional Data Transfer

- Used primarily in applications such as data transfer between two computers
- **Features**
 - Ports A can be configured as the bidirectional Port
 - Port B in Mode 0 or Mode 1.
 - Port A uses 5 Signals from Port C as handshake signals for data transfer
 - Remaining 3 Signals from Port C Used as – Simple I/O or handshake for Port B



THANK YOU