SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)

Coimbatore-35

DEPARTMENT OF BIOMEDICAL ENGINEERING

19BMB303 & Fundamentals of Microprocessors and Microcontrollers

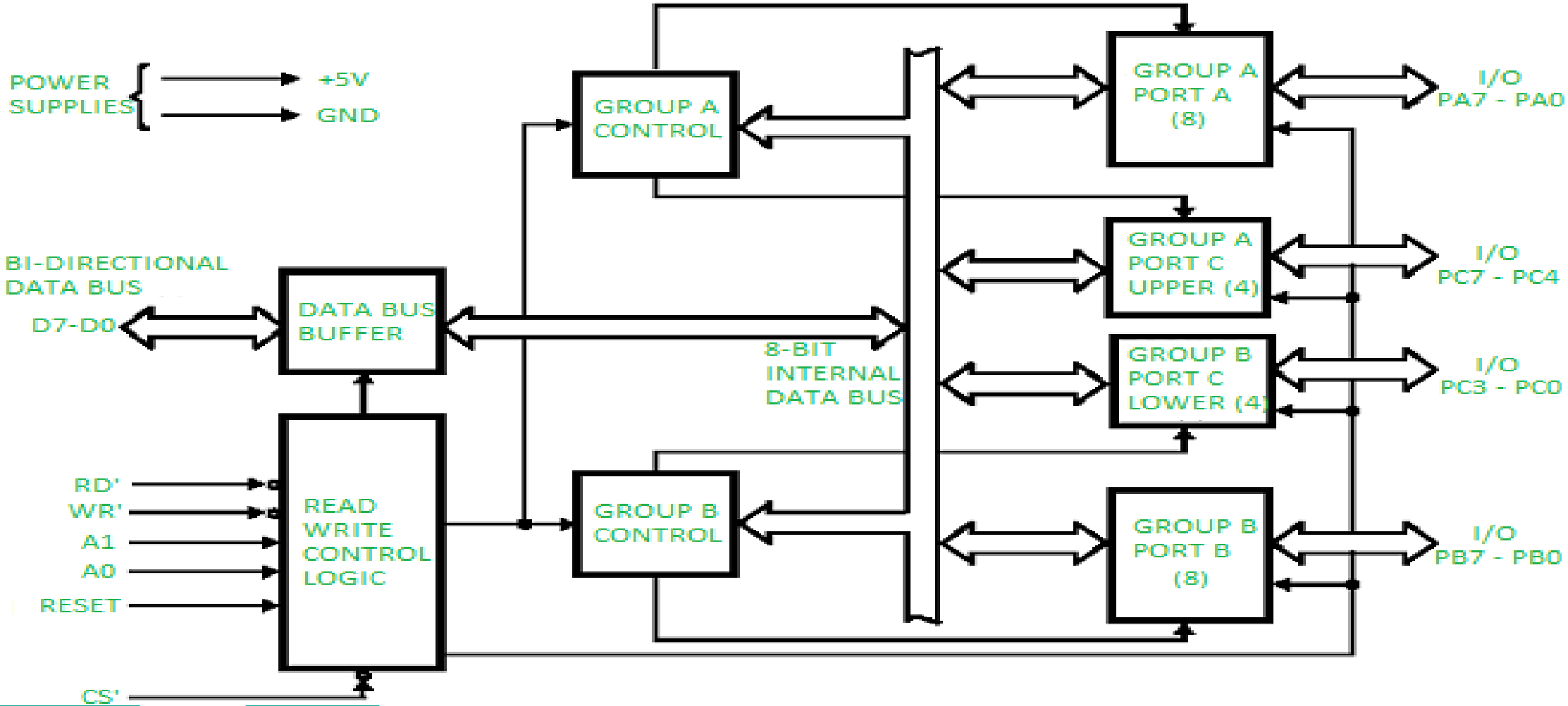
UNIT II – 8255 INTERFACING

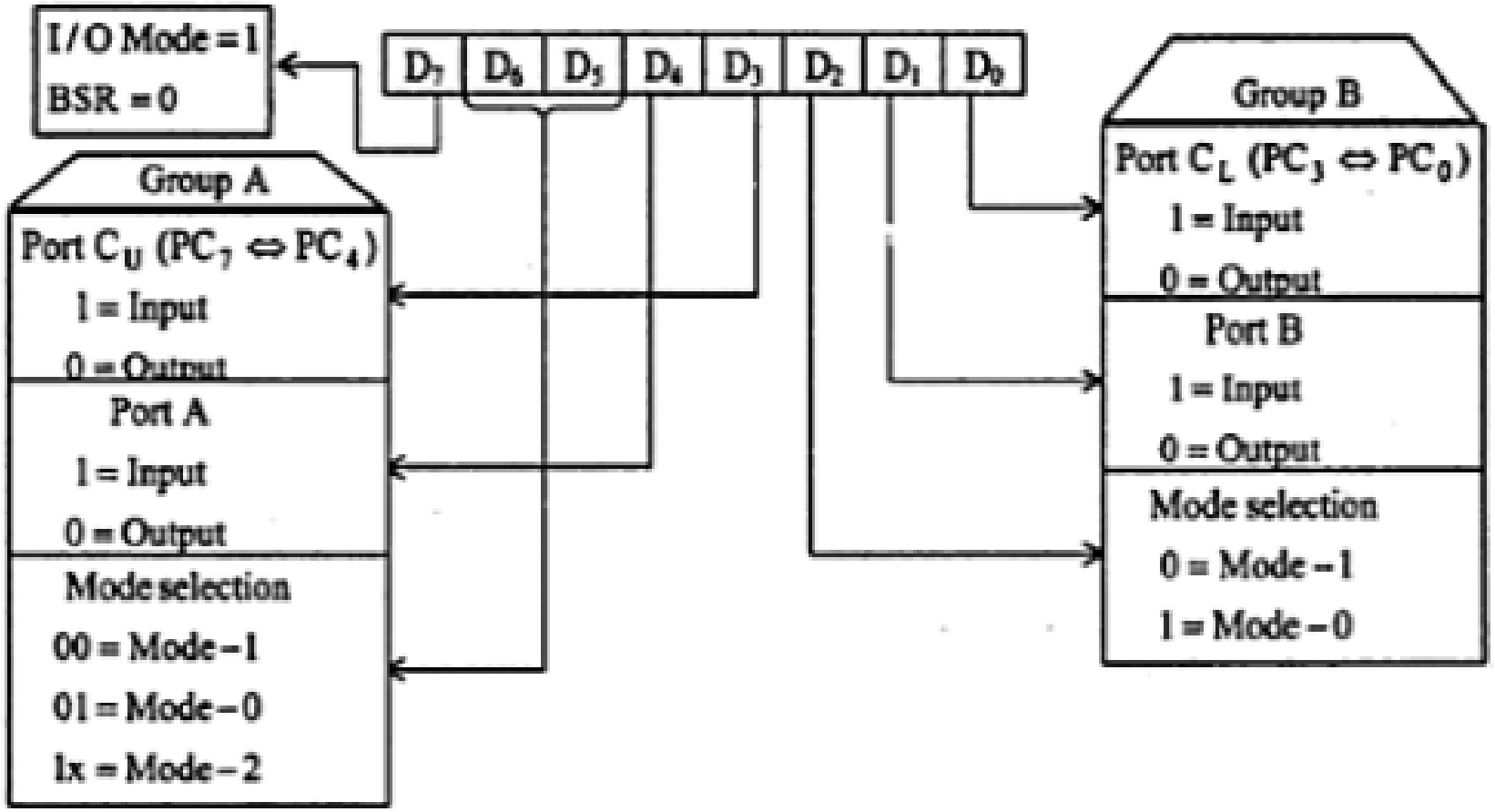
III Year/ VI Sem

Dr. K. Manoharan,
ASP / BME / SNSCT

8255 Interface

- The 8255 is a popular programmable peripheral interface chip developed by Intel.
- It's widely used in the design of microprocessor-based systems for interfacing various input and output devices.
- The 8255 is an 8-bit general purpose I/O (GPIO) chip.
- It consists of three 8-bit ports, labeled Port A, Port B, and Port C.


POWER SUPPLIES
+5V
GND
GROUP A CONTROL
GROUP A PORT A (8)
I/O PA7 - PA0
GROUP A PORT C UPPER (4)
I/O PC7 - PC4
BI-DIRECTIONAL DATA BUS
D7-D0
DATA BUS BUFFER
8-BIT INTERNAL DATA BUS
GROUP B PORT C LOWER (4)
I/O PC3 - PC0
RD'
WR'
A1
A0
RESET
READ WRITE CONTROL LOGIC
GROUP B CONTROL
GROUP B PORT B (8)
I/O PB7 - PB0
CS'



Control word with group defination

BSR Mode

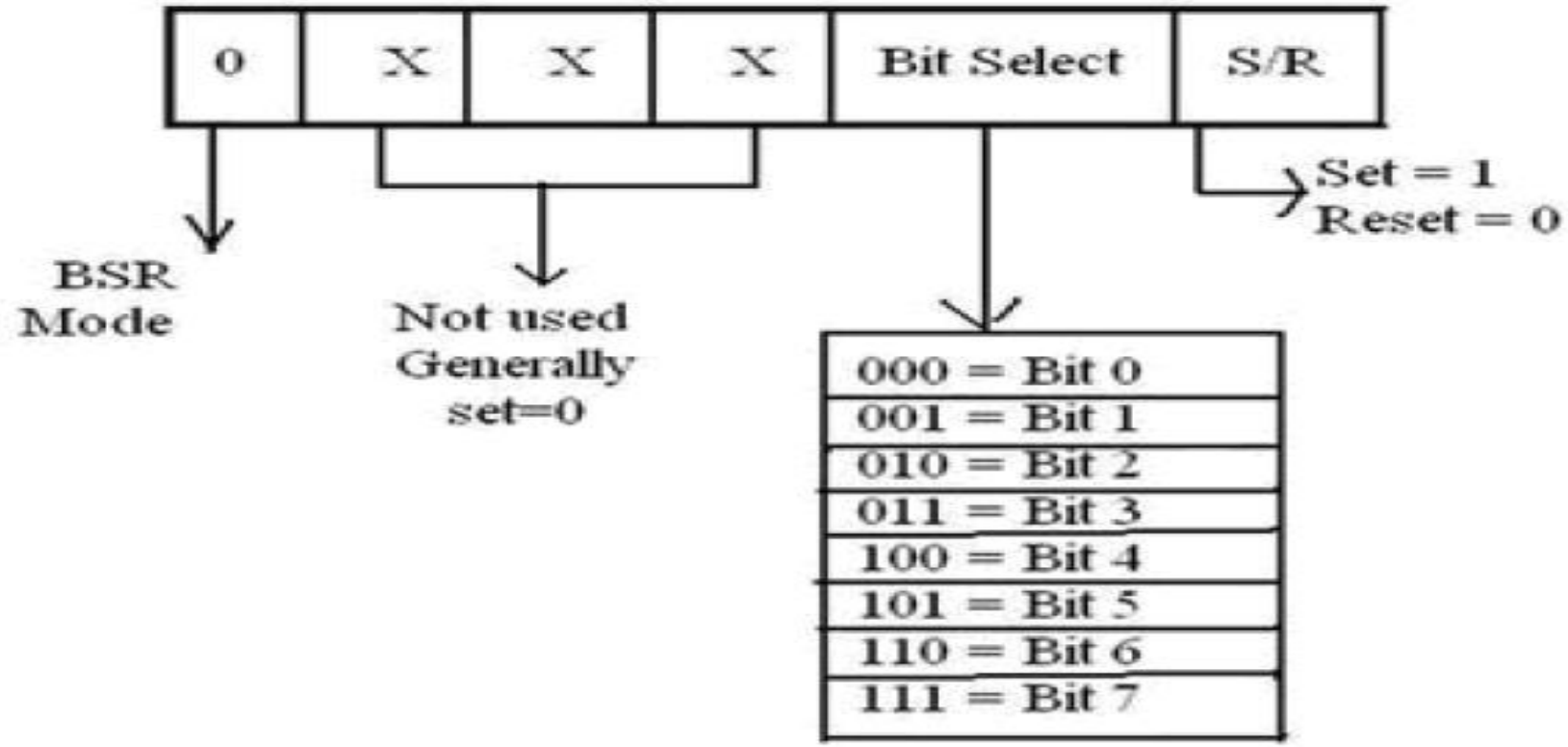
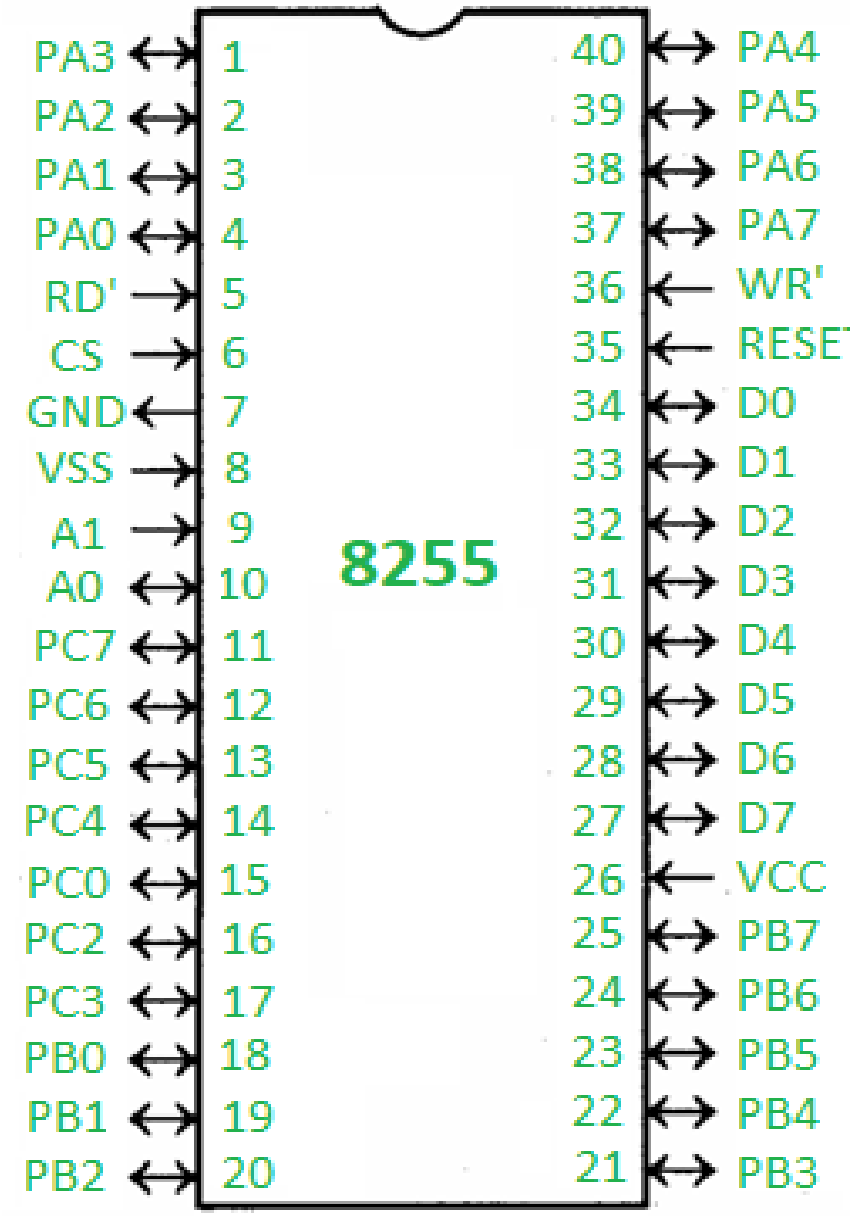


Fig. 6.3 BSR Mode of 8255


PA3 1
PA2 2
PA1 3
PA0 4
RD' 5
CS 6
GND 7
VSS 8
A1 9
A0 10
PC7 11
PC6 12
PC5 13
PC4 14
PC0 15
PC2 16
PC3 17
PB0 18
PB1 19
PB2 20
8255
40 PA4
39 PA5
38 PA6
37 PA7
36 WR'
35 RESE
34 D0
33 D1
32 D2
31 D3
30 D4
29 D5
28 D6
27 D7
26 VCC
25 PB7
24 PB6
23 PB5
22 PB4
21 PB3

- **Mode 0 –**In this mode all the three ports (port A, B, C) can work as simple input function or simple output function. In this mode there is no interrupt handling capacity.
- **Mode 1 –** Handshake I/O mode or strobbed I/O mode. In this mode either port A or port B can work as simple input port or simple output port, and port C bits are used for handshake signals before actual data transmission. It has interrupt handling capacity and input and output are latched.
- **Mode 2 –** Bi-directional data bus mode. In this mode only port A works, and port B can work either in mode 0 or mode 1. 6 bits port C are used as handshake signals. It also has interrupt handling capacity.

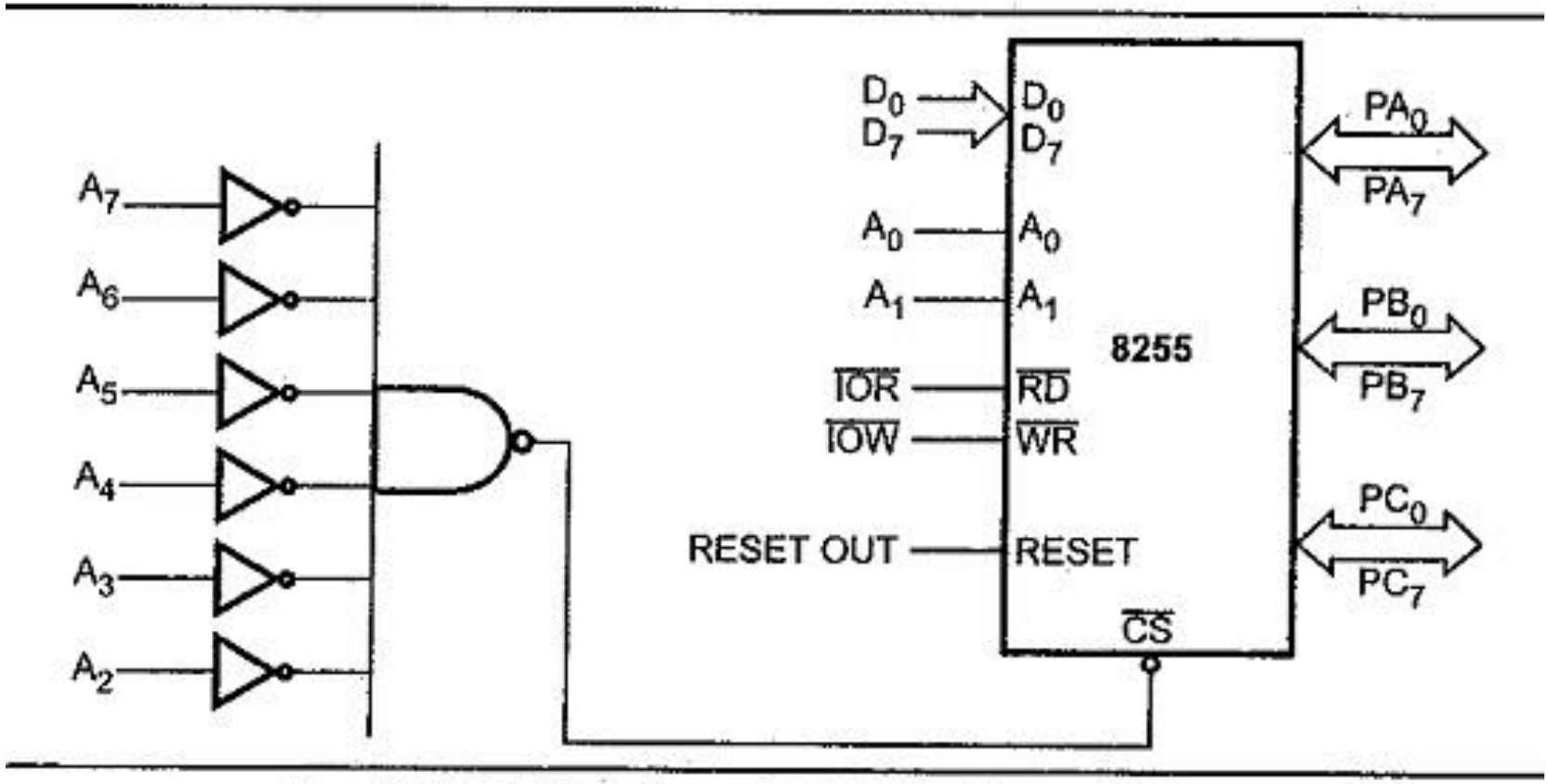


Fig. 14.17 Interfacing of 8255 in I/O mapped I/O

8251

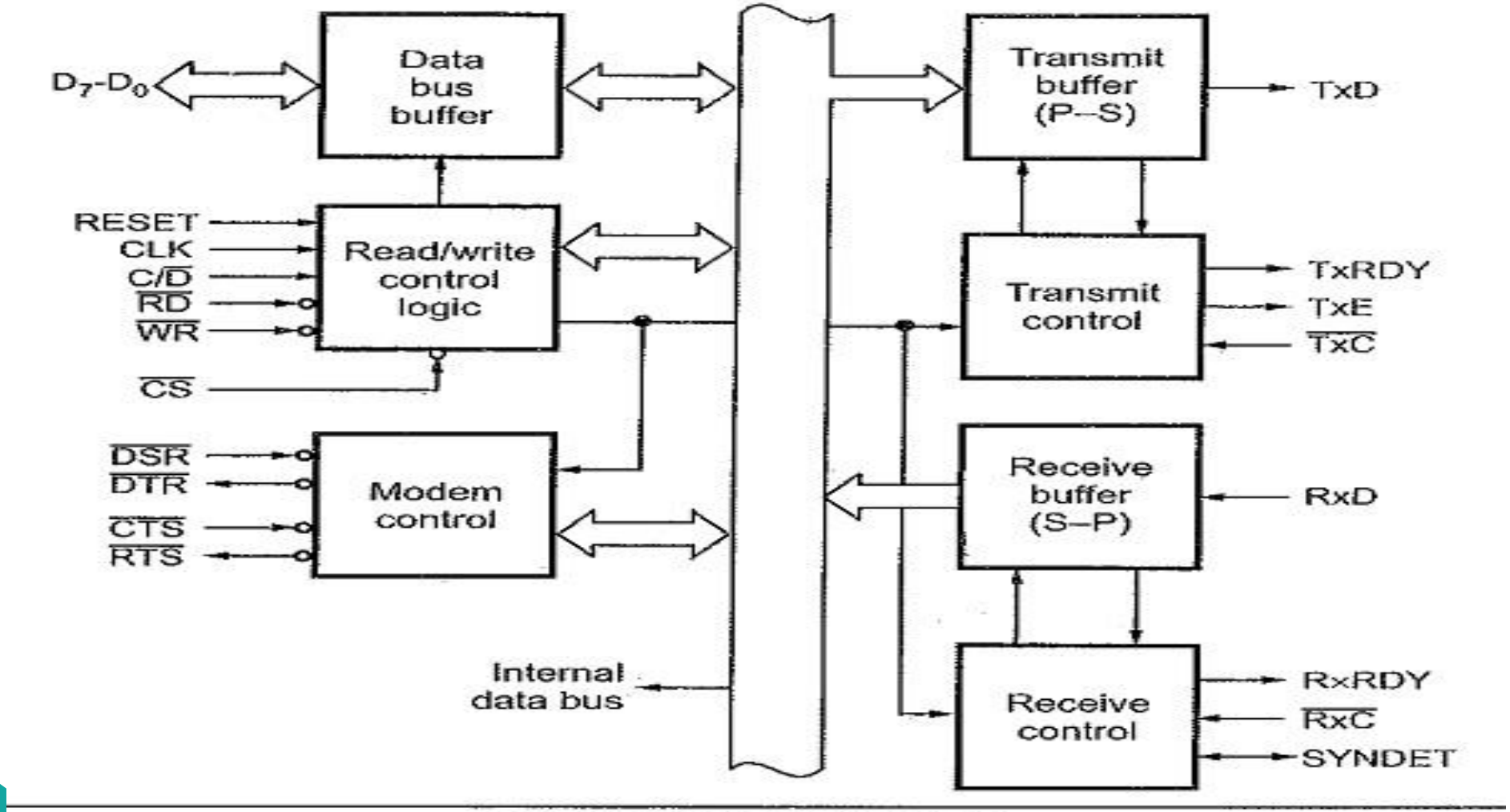


Fig. 14.37 Block diagram

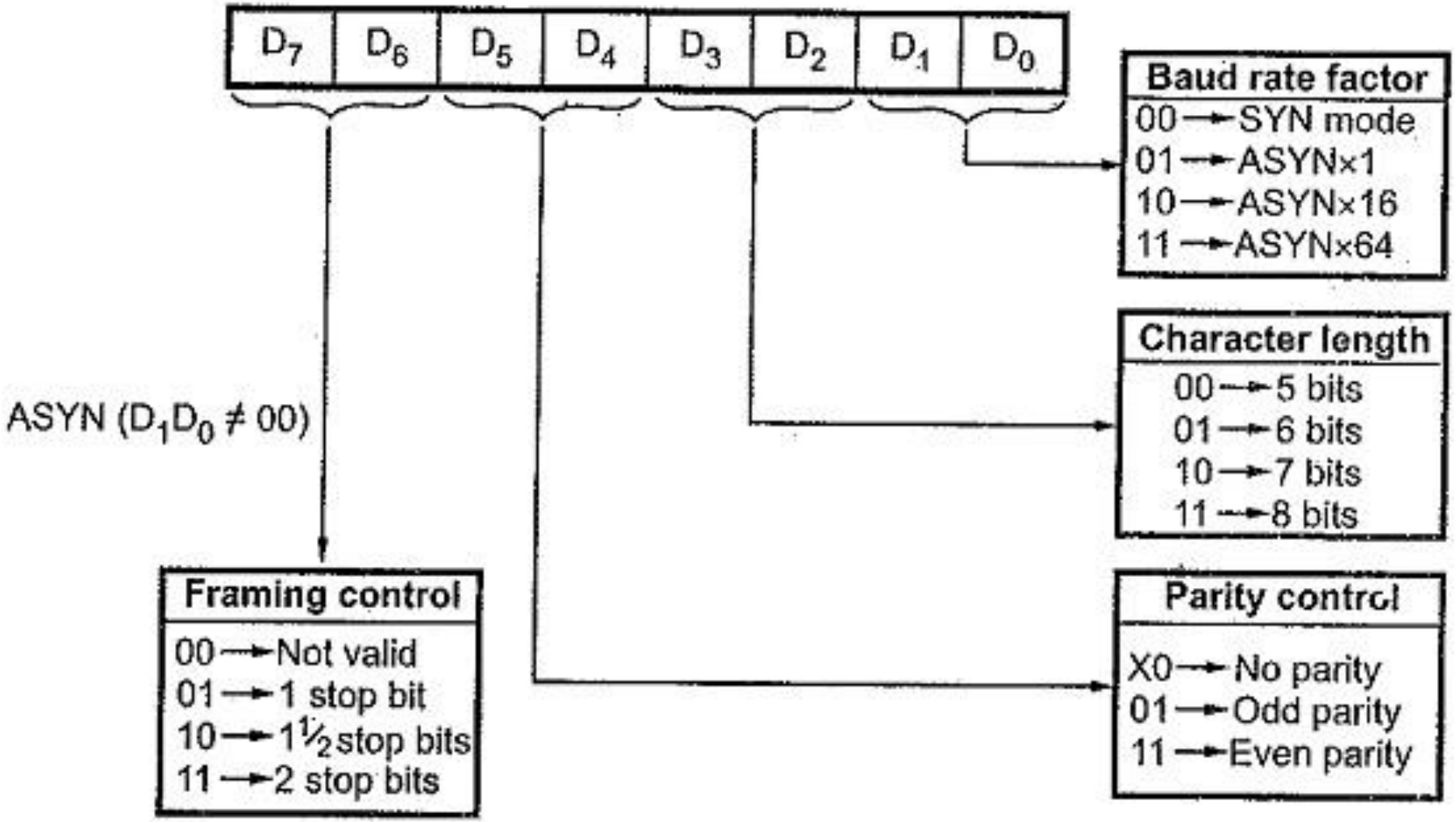


Fig. 14.38 Mode instruction format

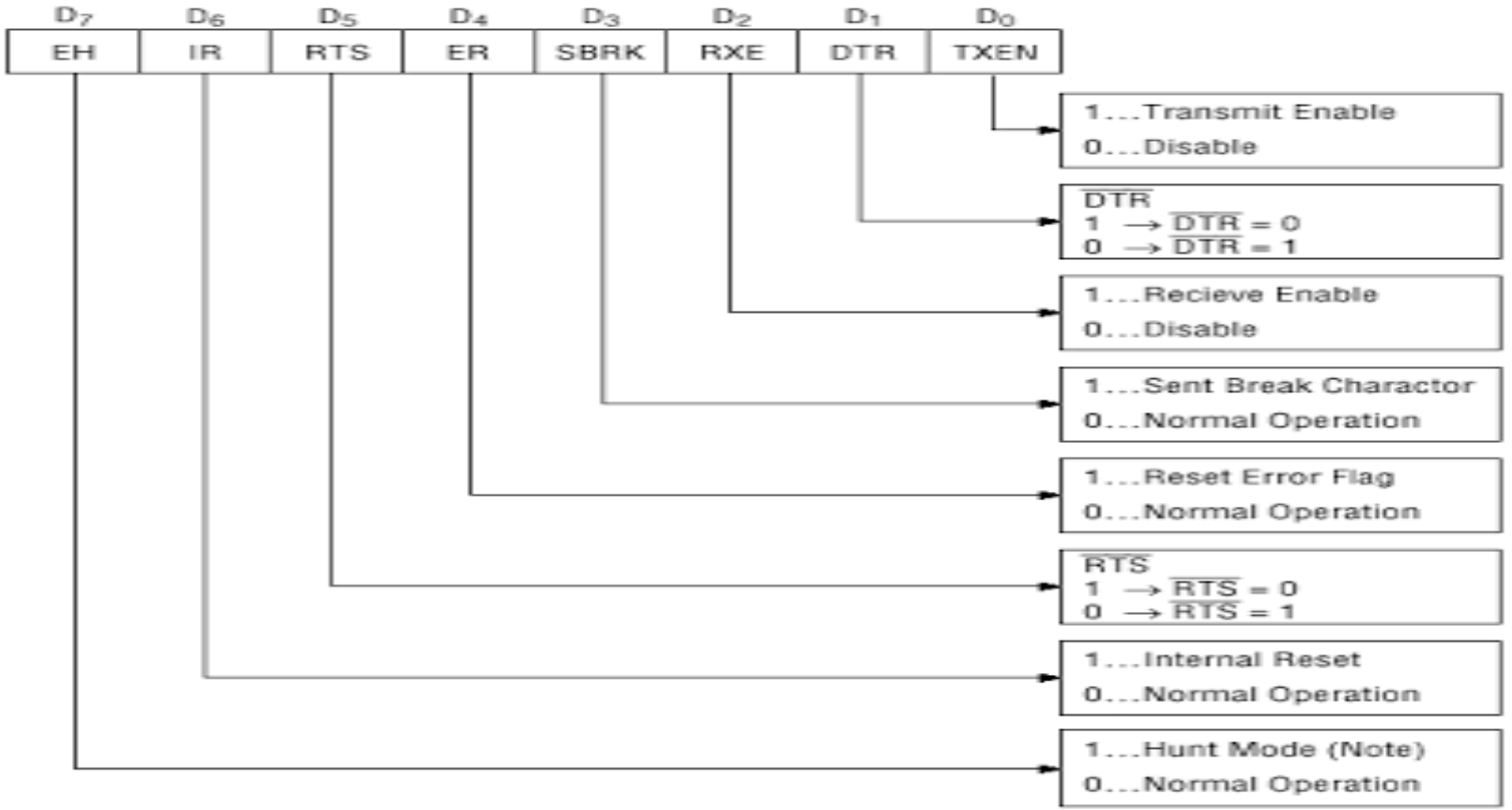


Fig. 4 Bit Configuration of Command

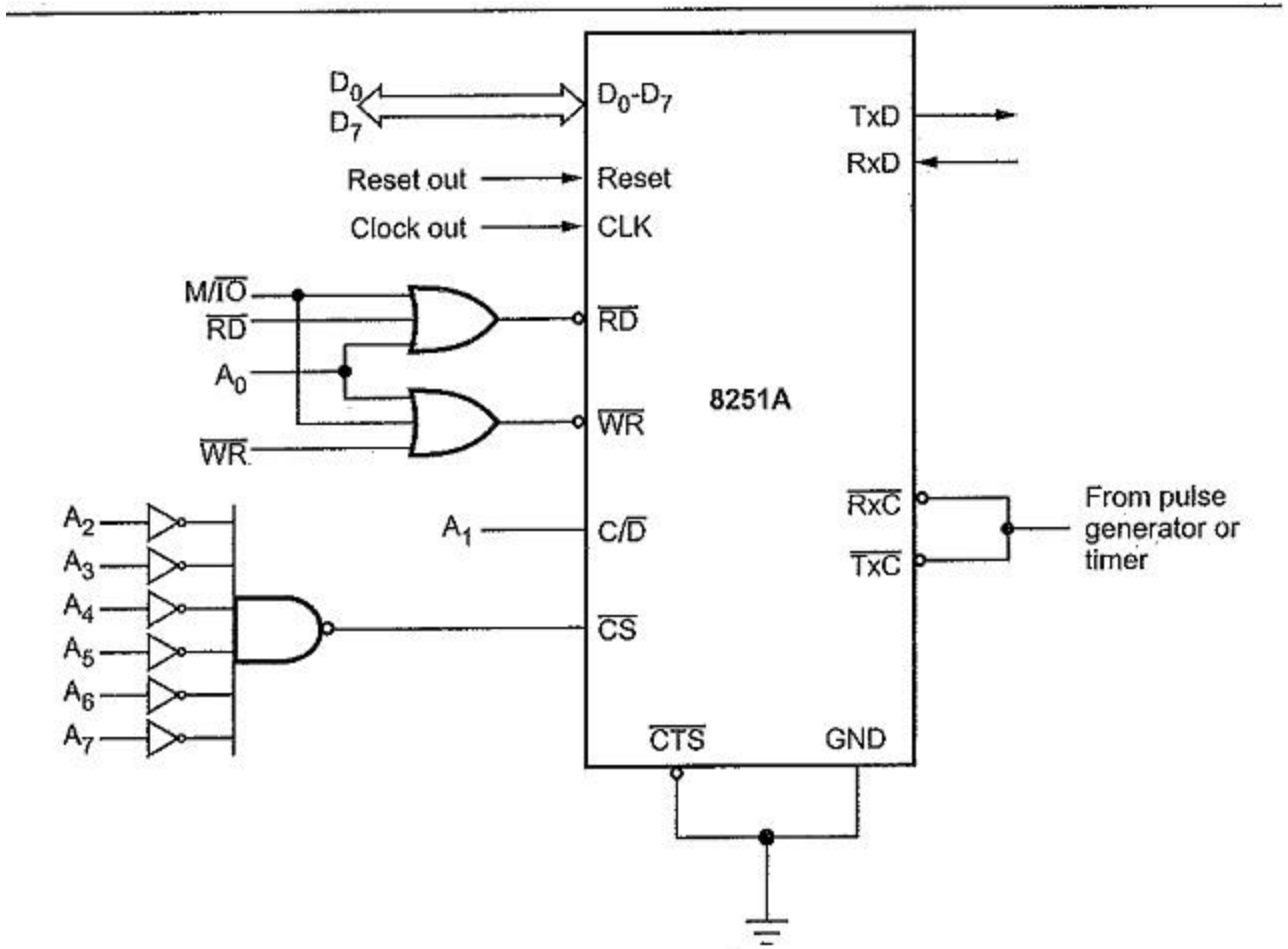


Fig. 14.46 Interfacing of 8251A with 8086 in I/O mapped I/O