Structural Units In Embedded Processor

- It internally connects all the structural units iñside the processor.
- Its width can be 8,16,32 or 64 bits

- It is the external bus that carries the address from the MAR to the memory as well as the IO devices and the other units of the system

- It is an external bus thet carries the data from or to the address

- It is an estema(bus to carry control) signal between the processor.and memory devices

- It is the interface unlt between the processor s internal units with the external buses

- Memory Address Register
- It holds the address of the byte or word to be fetched from external memories

- It holds the byte or word fetched from/to external memory or l/O address

Structural Units In Embedded Processor

- Program Counter
  - PC holds the memory address of the next instruction that would be executed.
- Stack Pointer
  - It is a pointer for an address which corresponds to stack top in the memory
- Instruction Register
  - Tt takes sequentially the instruction codes to the execution unit of the processor
- Instruction Decoder
  - It decodes the instruction opcode received at thR IR passes it to the processor CU
- Instruction Queue
  - It is the queue of instruction so that the IR does not have to wait for the next instruction after one has been carried out

Structural Units In Embedded Processor

- Arithmetic and Logical Unit
  - It is a unit to execute arithmetic and logical instruction according to the current instruction present in the IR
- Floating Point Processing Unit (FPPU)
  - A unit separate from ALU for floating point processing which is essential in processing mathematical functions fast in a microprocessor or DSP
- Floating Point Register Set(GPRS):
  - A register set dedicated for storing floating point number in a standard format and used bvFPPU for its data and stack

Structural Units In Embedded Processor

- Control Unit
  - It controls all the bus activities and unit functions needed for processing
- Memory management Unit (MMU)
  - It manages the memory such that instruction and data are readily available for processing
- Application Register Set
  - It is set of on-chip registers used during processing the instruction of the application program of the user

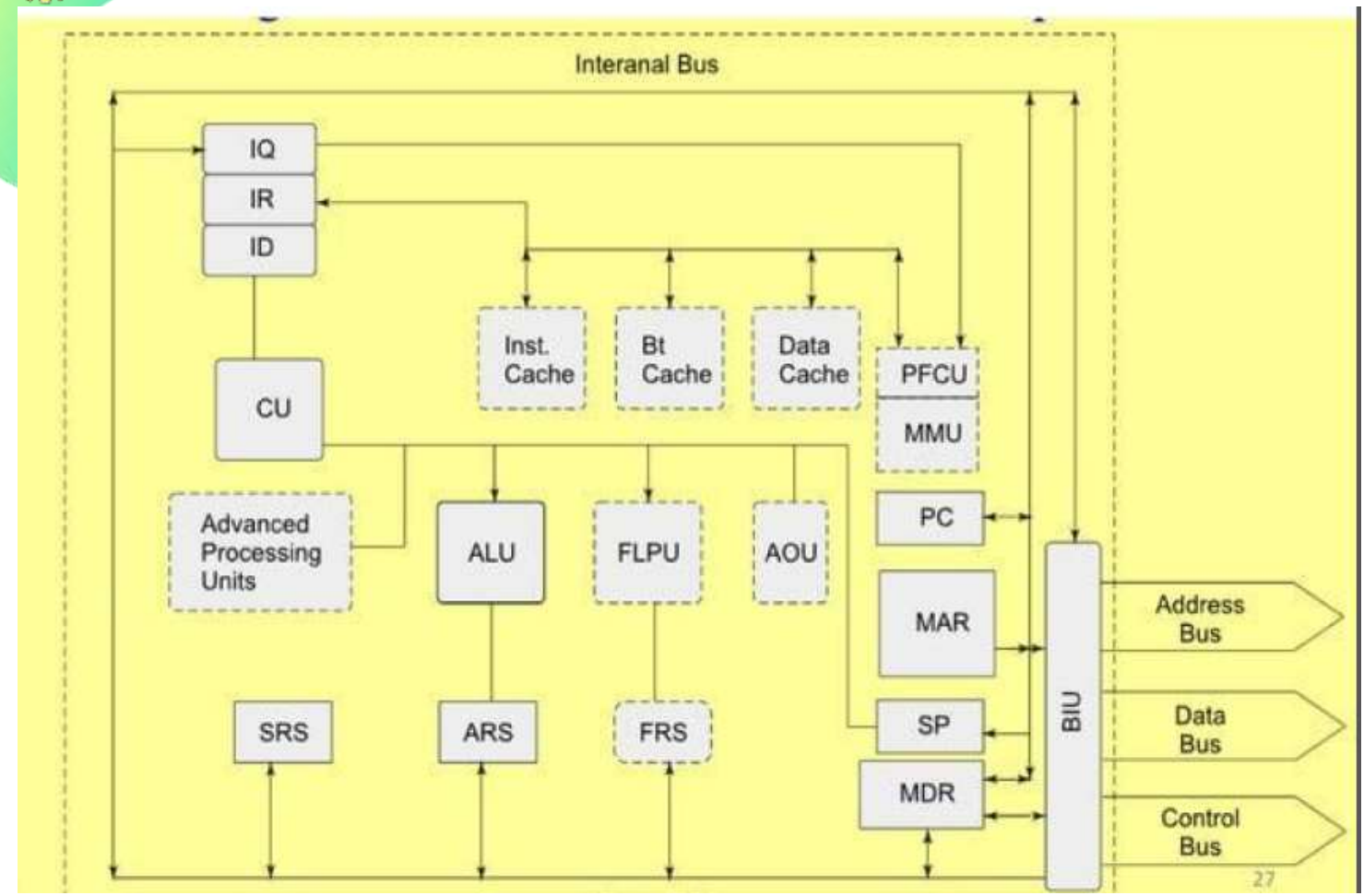
Structural Units In Embedded Processor

- Instruction Cache
  - It sequentially store s, like an Instruction queue, the instructions in FIFO.
- Data Cache
  - It stores the pre-fetched data from the external memory
  - The data cache generally holds both the key and the value together at the location

Pre-Fetch Control Unit

- It is the unit that controls the prefetching of data into the I-Cache and D-Cache in advance from the memory units
- The instruction and data are delivered when needed to the processor's execution unit

Structural Units In Embedded Processor



Structural Units In Embedded Processor

- Register Window

  - A register window consists of a subset of registers with each subset storing static variables and status words of a task or program thread.

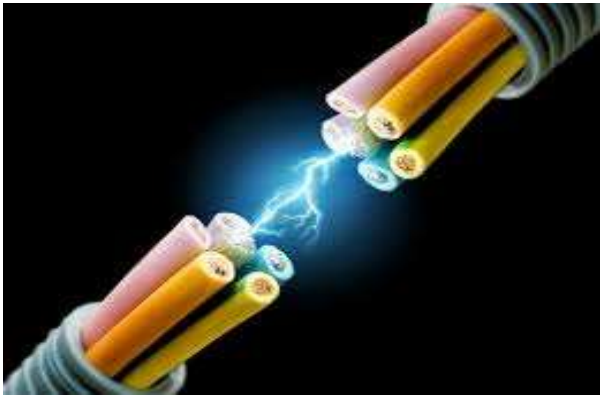
- Advanced processing Unit

  — These are units used for multi stage pipeline processing, multiline superscalar processing to obtain processing speed higher that one instruction per clock cycle

- Atomic Operations Unit (AOU):

  — It lets a user instruction when broken into number of processor instruction called atomic operation, finish before an interrupt of a process occurs.

RECAP….



…THANK YOU