SNS COLLEGE OF TECHNOLOGY

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

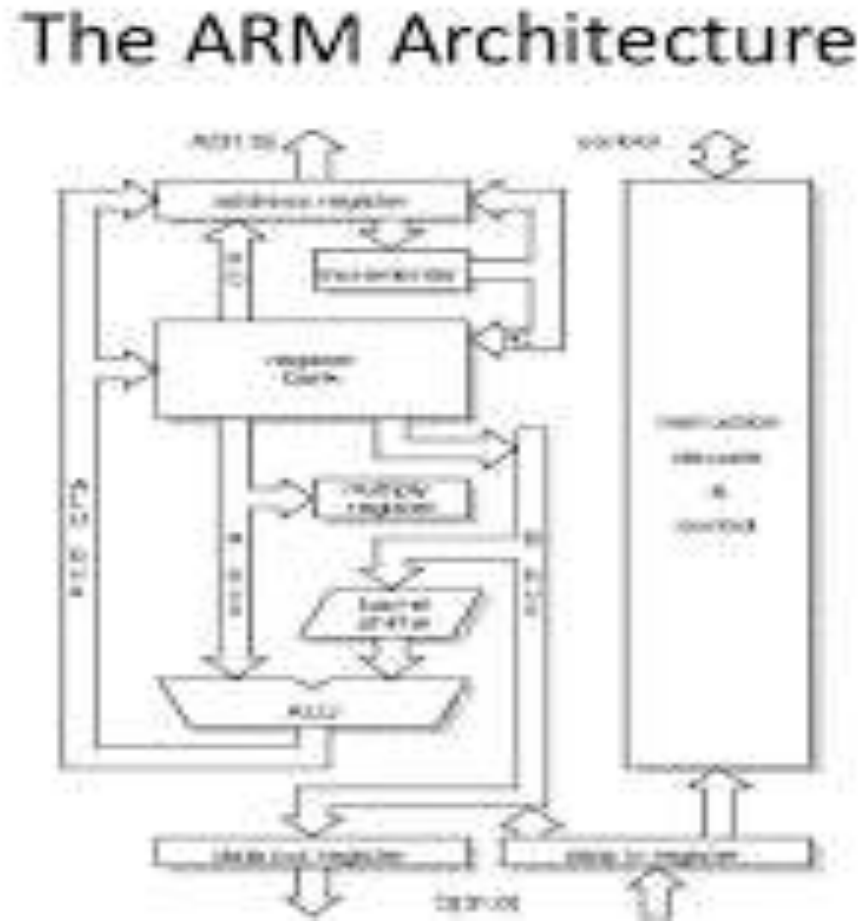
COURSE NAME: 19EEB303 / Microcontroller and its Applications

III YEAR / VI SEMESTER

Unit III – **IOT - ARCHITECTURE REFERENCE MODEL**

Topic:Architecture of ARM

ARM Architecture



ARM Architecture

The data flow diagram of the ARM core is shown in Figure, where the functional units are connected by data bus. The Arithmetic Logic Unit (ALU) and Multiply-Accumulate unit (MAC) retrieve value from data path A and B and store the answer back in the register file. One of the integral parts of the core is the Barrel Shifter (BS). Itis used in pre-processing the source operand Rm. The BS along with ALU is used in calculating many different expressions. The base address is generated by the ALU for the load and store instructions and stored in the address register. The core is capable of accessing an array of memory locations with help of the incrementer. It auto-increments, to access the next sequential memory location until an exception or interrupt changes the flow of execution.

ARM Architecture

The ARM has seven basic operating modes: six privileged mode and one non privileged mode (user). The privileged modes are used to service interrupt , exception and access protected resources.

User Mode : is an unprivileged mode under which most tasks run. This mode is used for executing application programs.

System mode : is a privileged mode to run user and system programs. Under this mode the user has all the access permissions. This mode uses the same set of registers as thenon privilegeduser mode.

ARM Architecture

Supervisor Mode: This is the mode where in the OS kernel operates. This mode is entered on reset and when a Software Interrupt instruction is executed.

Two of the privilege modes are allocated for interrupt handling. In general, ARM has two levels of interrupts.

Fast Interrupt Request (FIQ) : FIQ mode is entered when a high priority (fast) interrupt is raised. FIQ supports channel communication for data transfer.

ARM Architecture

Interrupt Request (IRQ) :IRQ isentered when a low priority (normal) interrupt is raised. This is a privileged mode for general purpose interrupt handling.

Abort : used to handle memory access violations. The abort mode handles data abort and pre-fetch abort.

Undefined : used to handle undefined instructions that are not supported by the implementation.

ARM Architecture

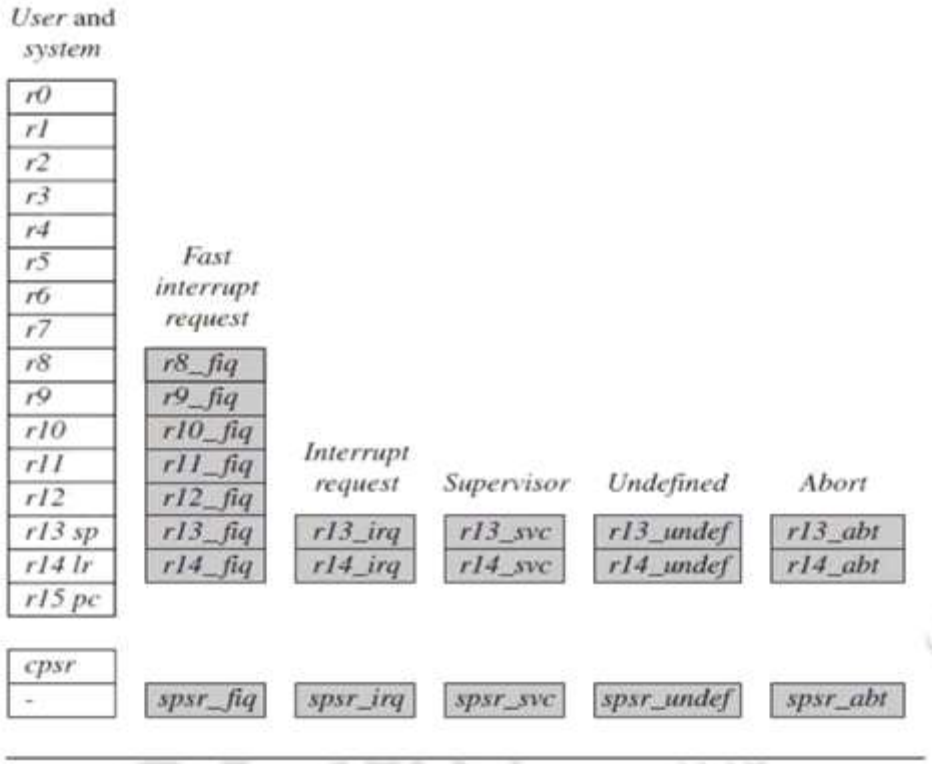


Figure 1.2Complete register set of ARM

ARM Architecture

Registers

- Arm has 37 registers, each 32 bits long.
- The registers are broadly classified into Special Purpose Registers(SPR) and General Purpose Registers(GPR).
- The SPRs are processor driven registers and GPRs are for the programmer. Overall there are about 18 active registers of which 16 registers r0 to r15 are visible to the user.
- In this the registers r13, r14 and r15 are used as the stack pointer, link register(lr) and program counter(pc) respectively.
- The lr is used to store the return address whenever the control shifts to the subroutine.
- There are two program status registers CPSR and SPSR (current program status register and saved program status register).
- Out of the 37 registers, 20 registers are used orthogonally under different banks.
- The processor mode decides which bank is accessible. The complete register set under different modes is shown in Figure 1.2.

ARM Architecture

The ARM Register Set

The shaded region in Figure 1.2 shows the way the registers are used for different privileged and non privileged modes. On the left is the user and system mode and on the right side the currently visible set of registers is shown for each privileged mode.All instructions can access GPRs and only a few instructions can access the SPRs. One of the prominent SPR is Program Status Register (PSR). The PSR in ARM represents the outcome of internal operations. It helps in monitoring the status of the processor. The PSR is generallyreferred to as Current PSR. There is another PSR for storage purpose calledSaved PSR (SPSR).The processor switches from one mode to another on demand of a interrupt, exception and privileged instruction.

ARM Architecture

As the processor transits via a privileged mode to non privileged mode vice versa,
the current executing mode CPSR is saved in the SPSR of the initiator mode.
After completion of the task, it moves back to the earlier switched mode.
This procedure is similar to context switching.
At the end a special return instruction it copies the SPSR into the CPSR.
The layout of the PSR is shown in figure 1.3. PSRs can be split into four 8-bit fields that can be individually written as:

ARM Architecture

Figure 1.3Current program status register

- Condition code flags
  - N = Negative result from ALU
  - Z = Zero result from ALU
  - C = ALU operation carried out
  - V = ALU operation overflowed
- Sticky Overflow flag - Q flag
  - Architecture 5TE/J only
  - Indicates if saturation has occurred
- J bit
  - Architecture 5TEJ only
  - J = 1: Processor in Jazelle state
- Interrupt Disable bits.
  - I = 1: Disables the IRQ.
  - F = 1: Disables the FIQ.
- T Bit
  - Architecture xT only
  - T = 0: Processor in ARM state
  - T = 1: Processor in Thumb state
- Mode bits
  - Specify the processor mode