



SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)



COIMBATORE-35

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

COURSE NAME: 19EEB303 / Microcontroller and its Applications

III YEAR / VI SEMESTER

Unit III – IOT - ARCHITECTURE REFERENCE MODEL

Topic:Memory organization



Memory organization



Memory organization

ARM Memory Organization

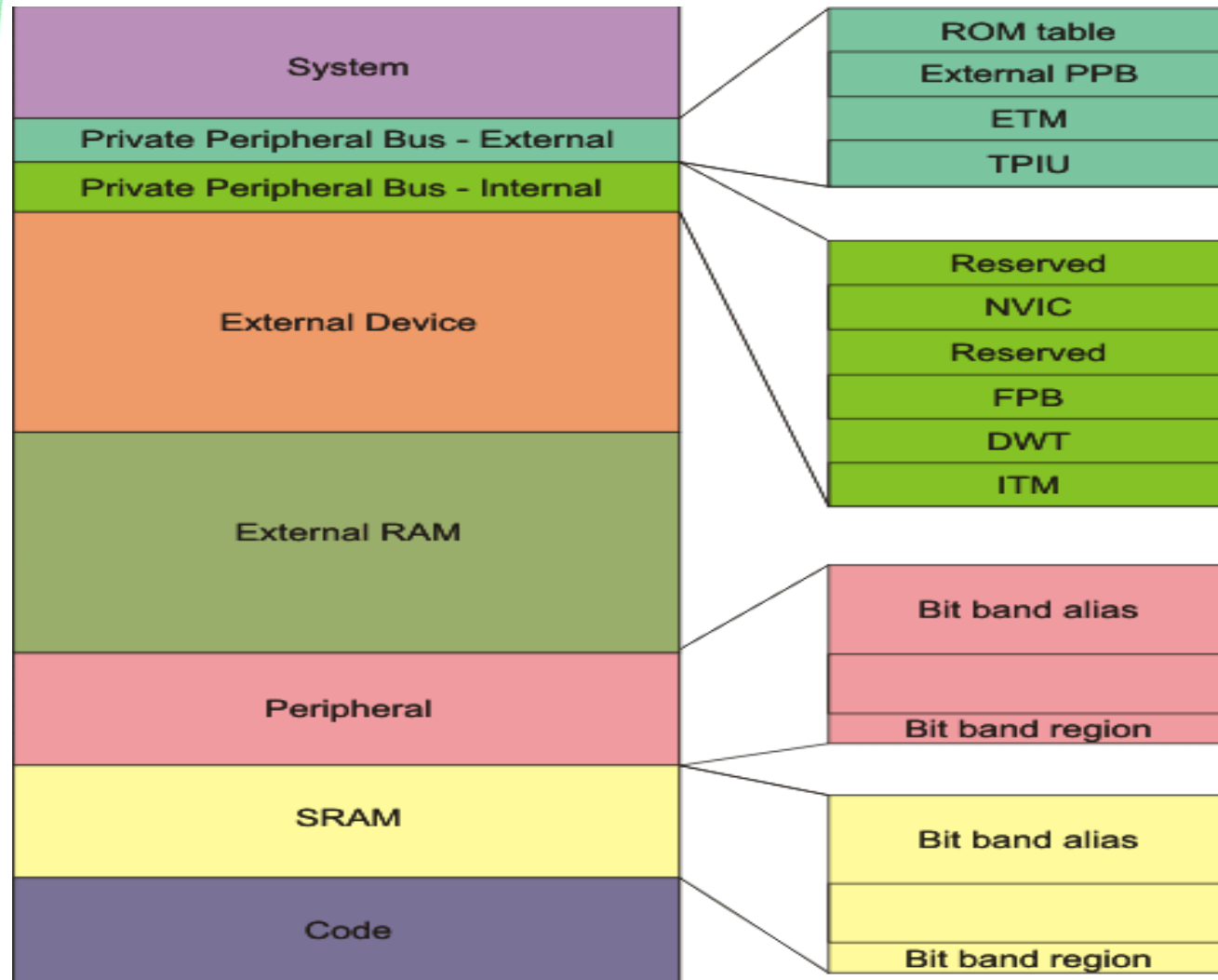
The Cortex-M3 and Cortex-M4 have a predefined memory map. This allows the built-in peripherals, such as the interrupt controller and the debug components, to be accessed by simple memory access instructions.

Thus, most system features are accessible in program code. The predefined memory map also allows the Cortex-M3 processor to be highly optimized for speed and ease of integration in system-on-a-chip (SoC) designs.

Overall, the 4 GB memory space can be divided into ranges as shown in picture below. The Cortex-M3 design has an internal bus infrastructure optimized for this memory usage.



Memory organization





Memory organization

The ARM Cortex-M3 memory is divided into following regions :

- **System** - .
- **Private Peripheral Bus - External** - Provides access to :
 - the Trace Port Interface Unit (TPIU),
 - the Embedded Trace Macrocell (ETM),
 - the ROM table,
 - implementation-specific areas of the PPB memory map.
- **Private Peripheral Bus - External** - Provides access to :
 - the Instrumentation Trace Macrocell (ITM),
 - the Data Watchpoint and Trace (DWT),
 - the Flashpatch and Breakpoint (FPB),
 - the System Control Space (SCS), including the MPU and the Nested Vectored Interrupt Controller (NVIC).



Memory organization

- **External Device** - This region is used for external device memory.
- **External RAM** - This region is used for data.
- **Peripheral** - This region includes bit band and bit band alias areas.
 - Peripheral Bit-band alias - Direct accesses to this memory range behave as peripheral memory accesses, but this region is also bit addressable through bit-band alias.
 - Peripheral bit-band region - Data accesses to this region are remapped to bit band region. A write operation is performed as read-modify-write.
- **SRAM** - This executable region is for data storage. Code can also be stored here. This region includes bit band and bit band alias areas.
 - SRAM Bit-band alias - Direct accesses to this memory range behave as SRAM memory accesses, but this region is also bit addressable through bit-band alias.
 - SRAM bit-band region - Data accesses to this region are remapped to bit band region. A write operation is performed as read-modify-write.
- **Code** - This executable region is for program code. Data can also be stored here.



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