SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)
COIMBATORE-35
Accredited by NBA-AICTE and Accredited by NAAC – UGC with A++ Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

19EEE305 / EMBEDDED SYSTEMS
III YEAR / VI SEMESTER

UNIT-II: HARDWARE ARCHITECTURE OF EMBEDDED SYSTEM

IIC

IIC – Inter Integrated Circuits

- I2C Bus developed by Philips Semiconductor for TV sets in the 1980's
- I2C is a 2 wire communication such as SDA (serial data) and SCL (serial clock).
- It performs half-duplex and synchronous communication.
- I2C Supports:
- 1. Master Mode 2. Slave Mode 3. Multi Master Mode

Contd.,

- Addressing is needed for each slave device. For example: In PIC microcontroller - MSSP Address Register is used for addressing.
- No chip select or Arbitration logic is required

IIC-Data Transfer

Sent by Master

Sent by Slave

Fig. Data Transfer from Master to slave

Sent by Master

Sent by Slave

Fig. Data Transfer from Slave to Master

Contd.,

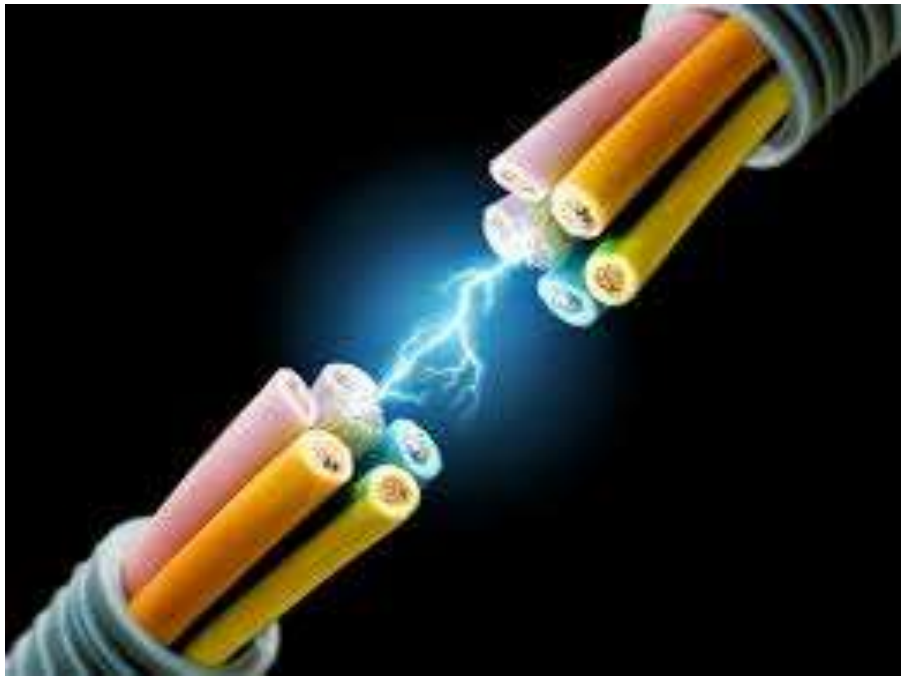
Steps:

- Master sends start condition (S) and controls the clock signal.
- Master sends a unique 7-bit slave device address.
- Master sends read / write bit (R/W) as 0 for slave receive and 1 for slave transmit.
- Wait for (or) send an acknowledge bit (A).
- Send (or) receive the data byte (8 bits) (DATA).
- Expect / send acknowledge bit (A)
- Send the stop bit (P).

IIC Application

•Used as a control interface to signal processing devices that has separate data interfaces.
•Example RF tuners, video decoders and encoders and Audio processor

RECAP….



…THANK YOU