SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)
COIMBATORE-35
Accredited by NBA-AICTE and Accredited by NAAC – UGC with A++ Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

19EEE305 / EMBEDDED SYSTEMS
III YEAR / VI SEMESTER

UNIT-II: HARDWARE ARCHITECTURE OF EMBEDDED SYSTEM

UART

UART

Baud Rate: It is assumed that the receiver knows how fast each bit is being transmitted. This transmission rate is known as the baud rate. The term

- Baud‖ is spelled only in the asynchronous communication.

UART Mode is as Follows:

- Non return to zero (NRZ) state denotes logic state is 1 at serial line.
- Start of serial bits is signaled by 1 to 0 transitions on the line for a period equal to reciprocal of baud rate.
- Transmission of a byte consists of one start bit, eight data bits, one parity bit and one stop bit

UART

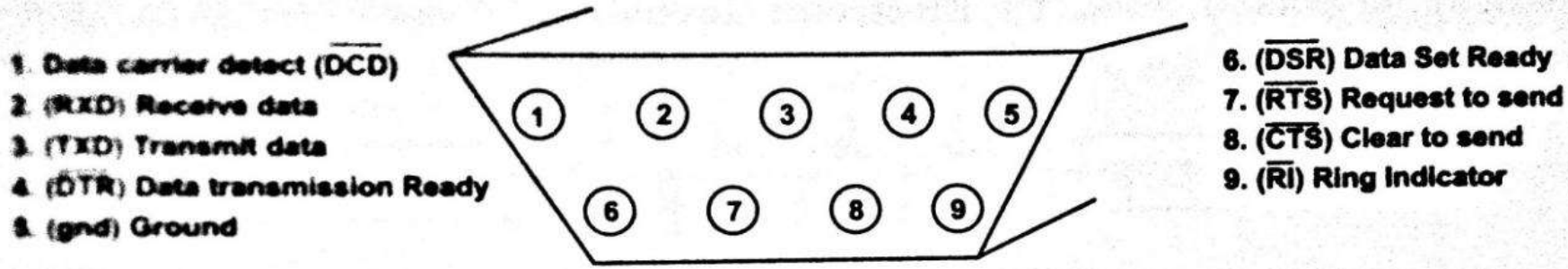


Fig. DB9 RS232-C

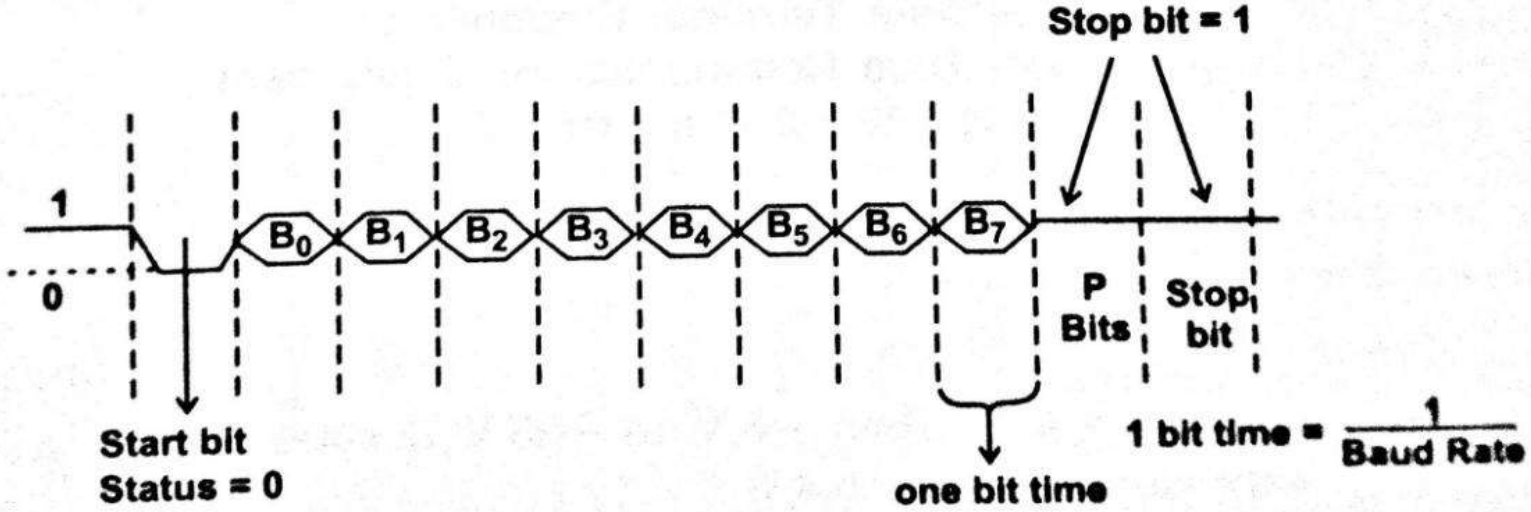
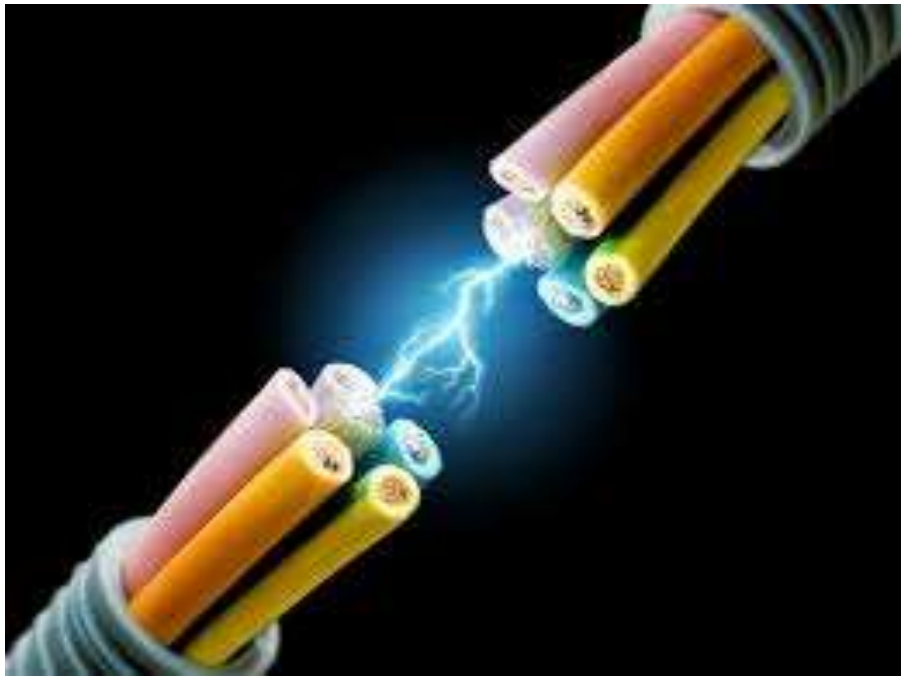


Fig. Transmission of bits

UART

- Stop bit is denoted by the logic one.
- 1 bit time = δT
- Therefore 10 bit time = 10δT
- Programmable bit (P.bit) is used for parity detection (or) to specify the purpose of serial data bits.
- For transmission and reception, UART 16550 has a 16 byte FIFO buffer

RECAP….



…THANK YOU