



SNS COLLEGE OF TECHNOLOGY
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sns
INSTITUTIONS

DEPARTMENT OF BIOMEDICAL ENGINEERING

8051 Architecture

III Year/ VI Sem

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ASP / BME / SNSCT



8051 Basic Component

- 4K bytes internal ROM
- 128 bytes internal RAM
- Four 8-bit I/O ports (P0 - P3).
- Two 16-bit timers/counters
- One serial interface

CPU	RAM	ROM
I/O Port	Timer	Serial COM Port

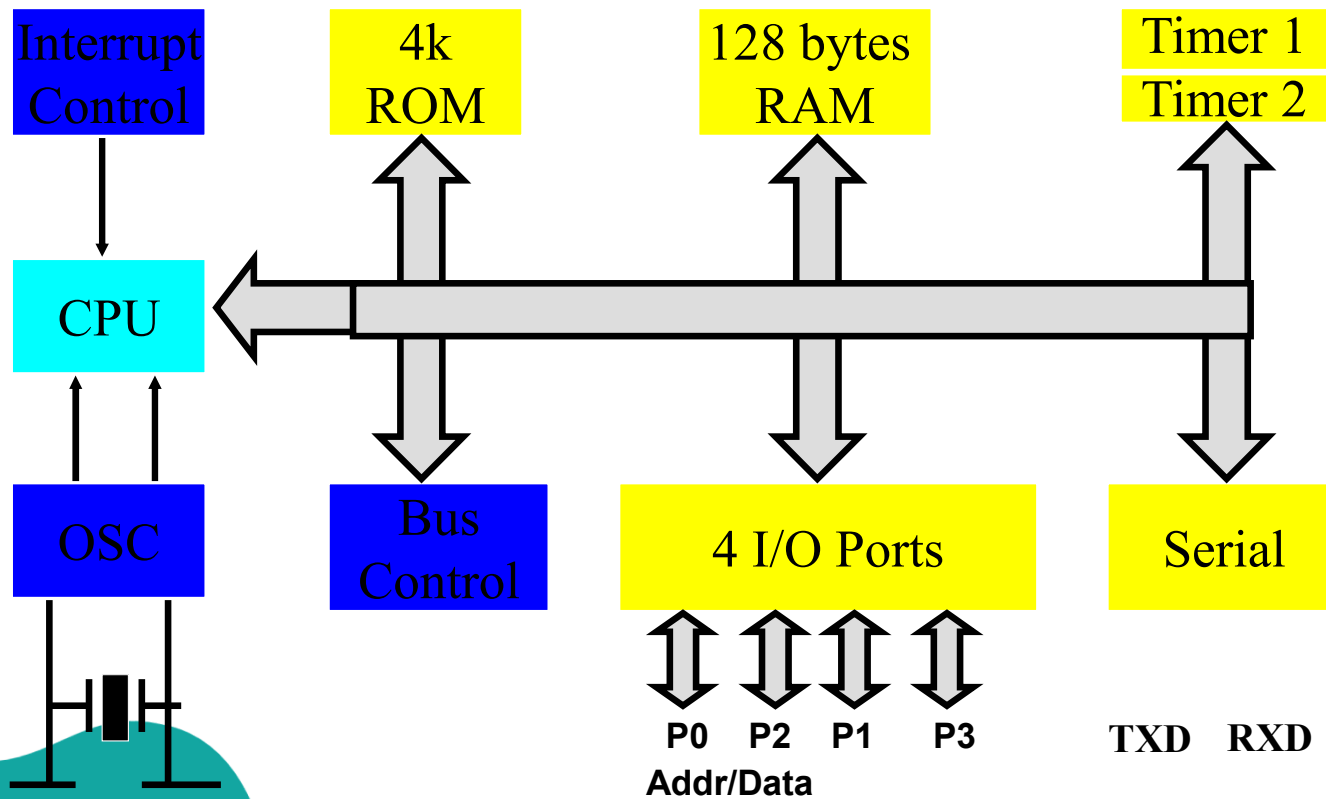
A single chip
Microcontroller





Block Diagram

External Interrupts



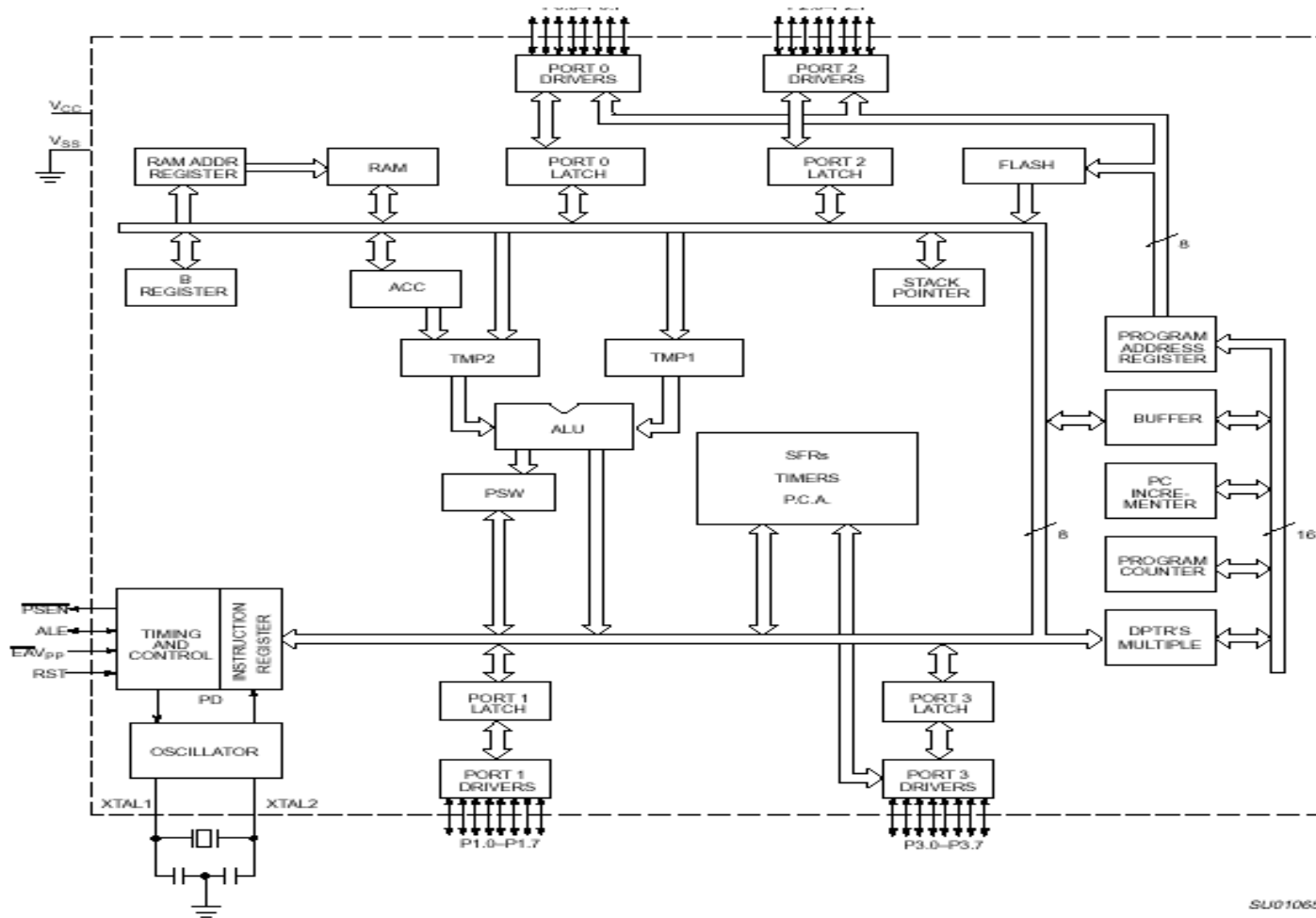


Other 8051 featur

- only 1 On chip oscillator (external crystal)
- 6 interrupt sources (2 external , 3 internal, Reset)
- 64K external code (program) memory(only read)PSEN
- 64K external data memory(can be read and write) by RD,WR
- Code memory is selectable by EA (internal or external)
- We may have External memory as data and code



8051 Internal Block Diagram





PSW: PROGRAM STATUS WORD. BIT ADDRESSABLE.

CY	AC	F0	RS1	RS0	OV	—	P
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CY	PSW.7	Carry Flag.
AC	PSW.6	Auxiliary Carry Flag.
F0	PSW.5	Flag 0 available to the user for general purpose.
RS1	PSW.4	Register Bank selector bit 1 (SEE NOTE 1).
RS0	PSW.3	Register Bank selector bit 0 (SEE NOTE 1).
OV	PSW.2	Overflow Flag.
—	PSW.1	User definable flag.
P	PSW.0	Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of '1' bits in the accumulator.

NOTE:

1. The value presented by RS0 and RS1 selects the corresponding register bank.

RS1	RS0	Register Bank	Address
0	0	0	00H-07H
0	1	1	08H-0FH
1	0	2	10H-17H
1	1	3	18H-1FH

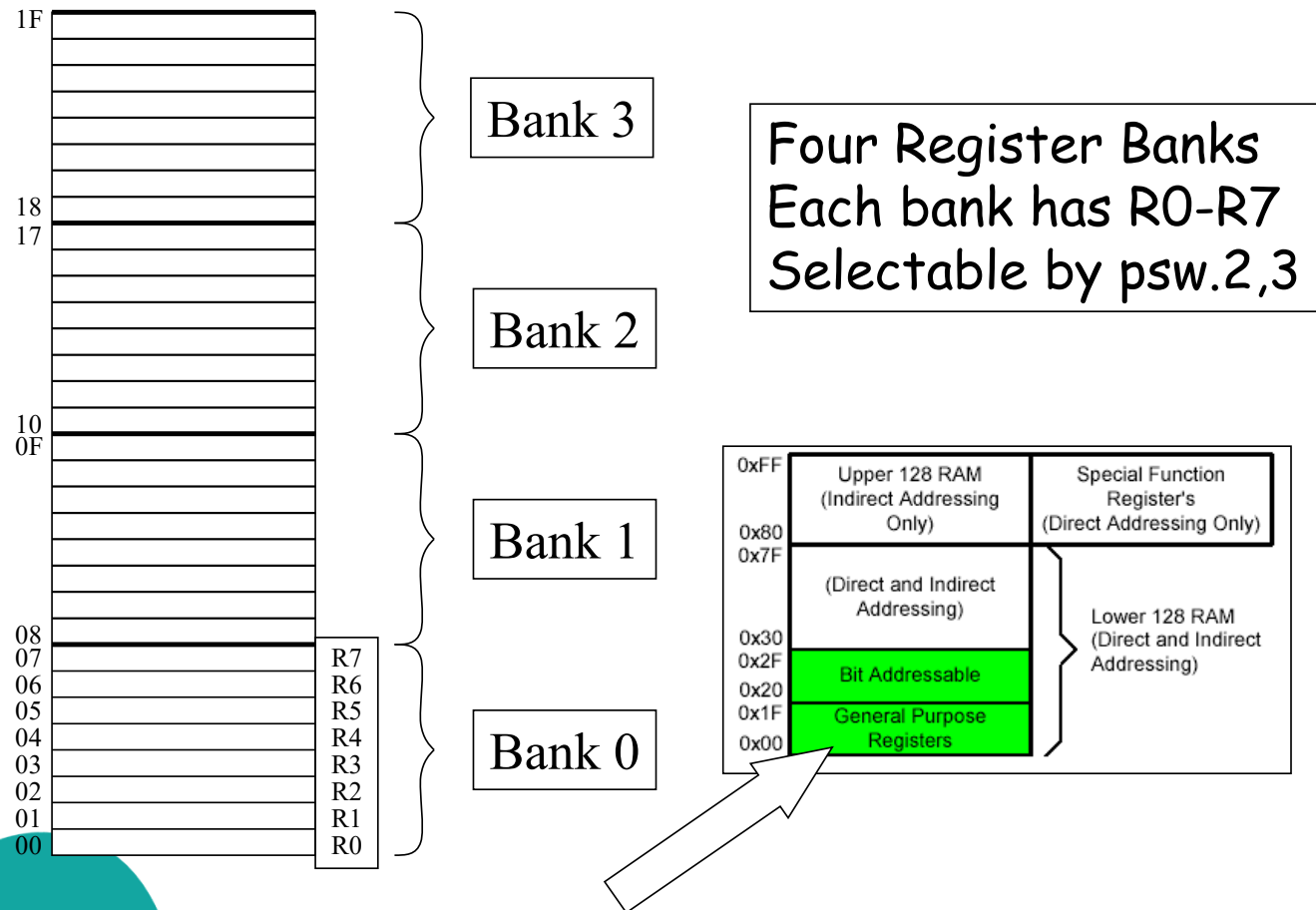


On-Chip Memory Internal RAM

0xFF	Upper 128 RAM (Indirect Addressing Only)	Special Function Register's (Direct Addressing Only)
0x80		
0x7F	(Direct and Indirect Addressing)	Lower 128 RAM (Direct and Indirect Addressing)
0x30		
0x2F	Bit Addressable	
0x20		
0x1F	General Purpose Registers	
0x00		



Registers





Bit Addressable Memory

2F	7F								78
2E									
2D									
2C									
2B									
2A									
29									
28									
27									
26									
25									
24									
23								1A	
22									10
21	0F								08
20	07	06	05	04	03	02	01	00	

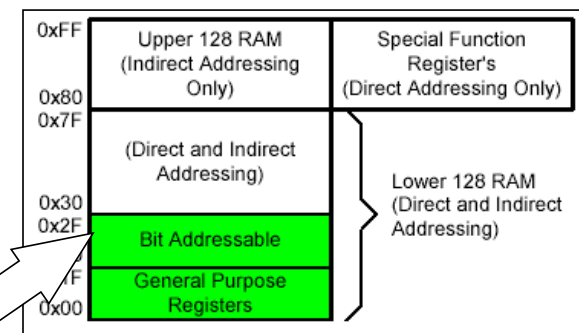
20h – 2Fh (16 locations X
8-bits = 128 bits)

Bit addressing:

mov C, 1Ah

or

mov C, 23h.2





Bit Addressable RAM

RAM

Byte address	Bit address							
27	3F	3E	3D	3C	3B	3A	39	38
26	37	36	35	34	33	32	31	30
25	2F	2E	2D	2C	2B	2A	29	28
24	27	26	25	24	23	22	21	20
23	1F	1E	1D	1C	1B	1A	19	18
22	17	16	15	14	13	12	11	10
21	0F	0E	0D	0C	0B	0A	09	08
20	07	06	05	04	03	02	01	00
1F	Bank 3							
18								
17	Bank 2							
10								
0F	Bank 1							
08								
07	Default register bank for R0–R7							
00								

Bit-addressable locations

Byte address	Bit address							
7F	General purpose RAM							
30								
2F								
2E								
2D								
2C								
2B								
2A								
29								
28								
27								
26								
25								
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21								
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Bit-addressable locations