SNS COLLEGE OF TECHNOLOGY
( An Autonomous Institution)
Coimbatore-35

DEPARTMENT OF BIOMEDICAL ENGINEERING

# 8051 Architecture

III Year/ VI Sem

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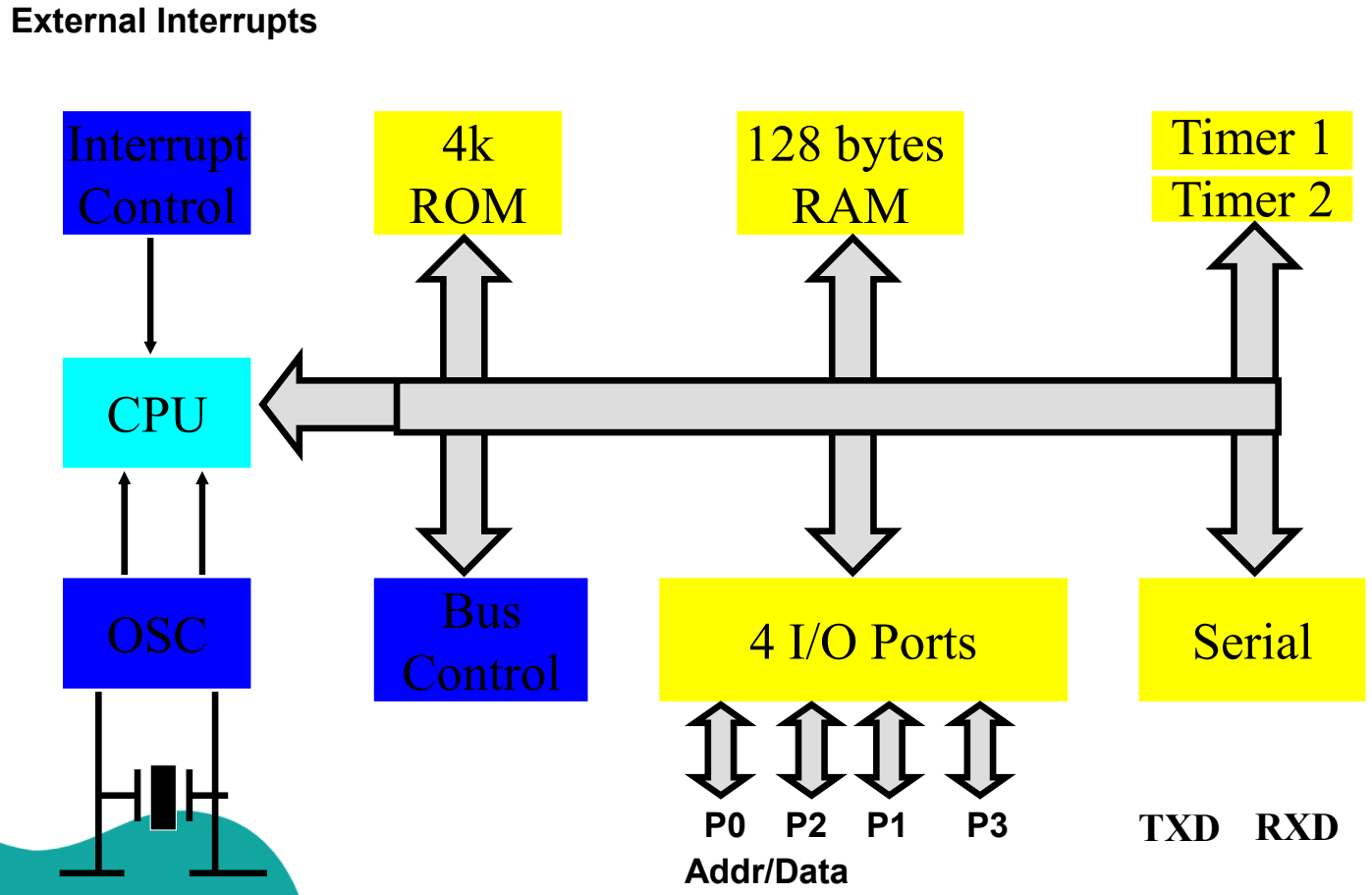
# 8051 Basic Component

- 4K bytes internal ROM
- 128 bytes internal RAM
- Four 8-bit I/O ports (P0 - P3).
- Two 16-bit timers/counters
- One serial interface

| CPU | RAM | ROM |
|---|---|---|
| I/O Port | Timer | Serial COM Port |

A single chip Microcontroller

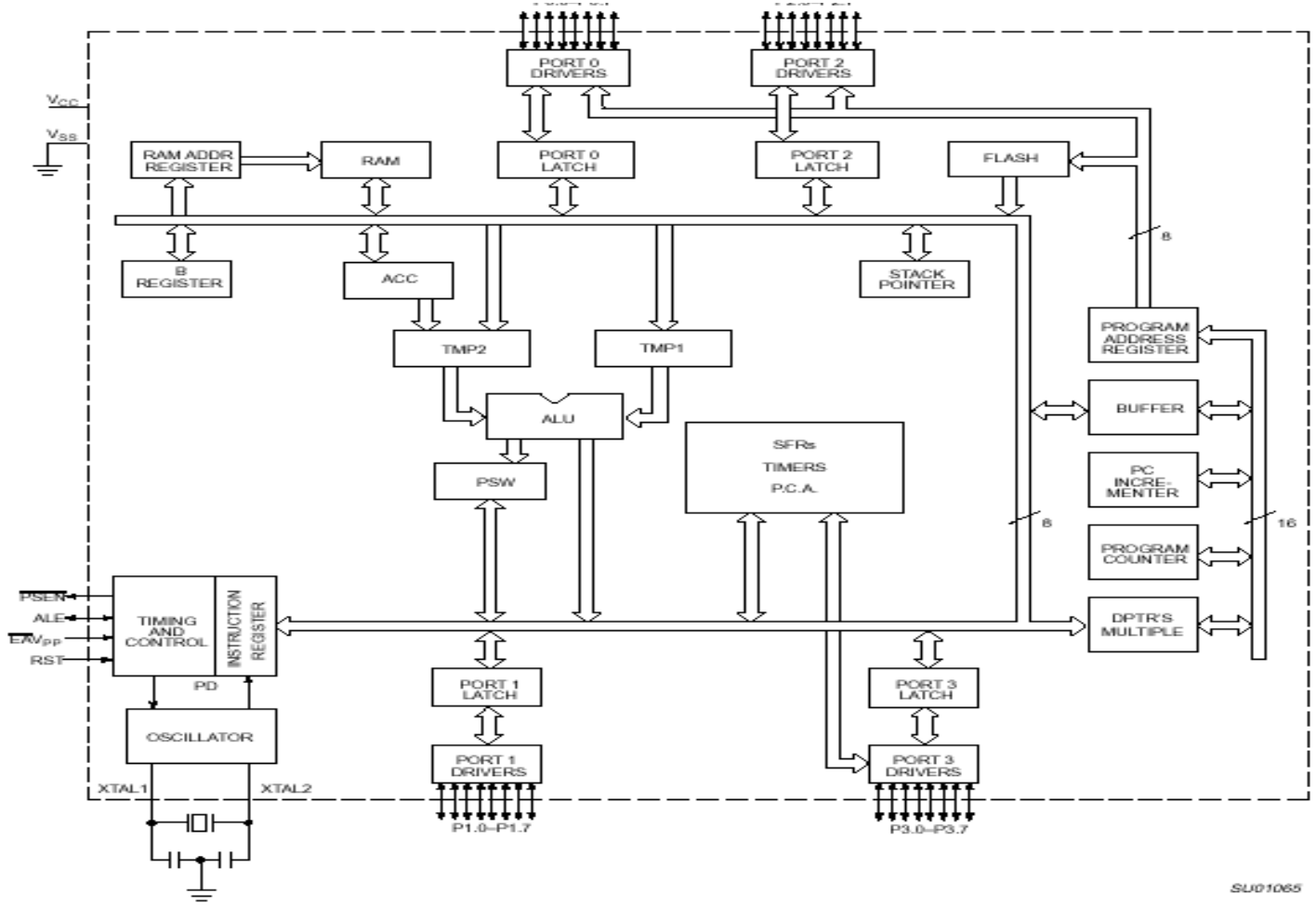
# Block Diagram



# Other 8051 featurs

- only 1 On chip oscillator (external crystal)
- 6 interrupt sources (2 external , 3 internal,  Reset)
- 64K external code (program) memory(only read)PSEN
- 64K external data memory(can be read and write) by RD,WR
- Code memory is selectable by EA (internal or external)
- We may have External memory as data and code

# 8051 Internal Block Diagram



## PSW: PROGRAM STATUS WORD. BIT ADDRESSABLE.

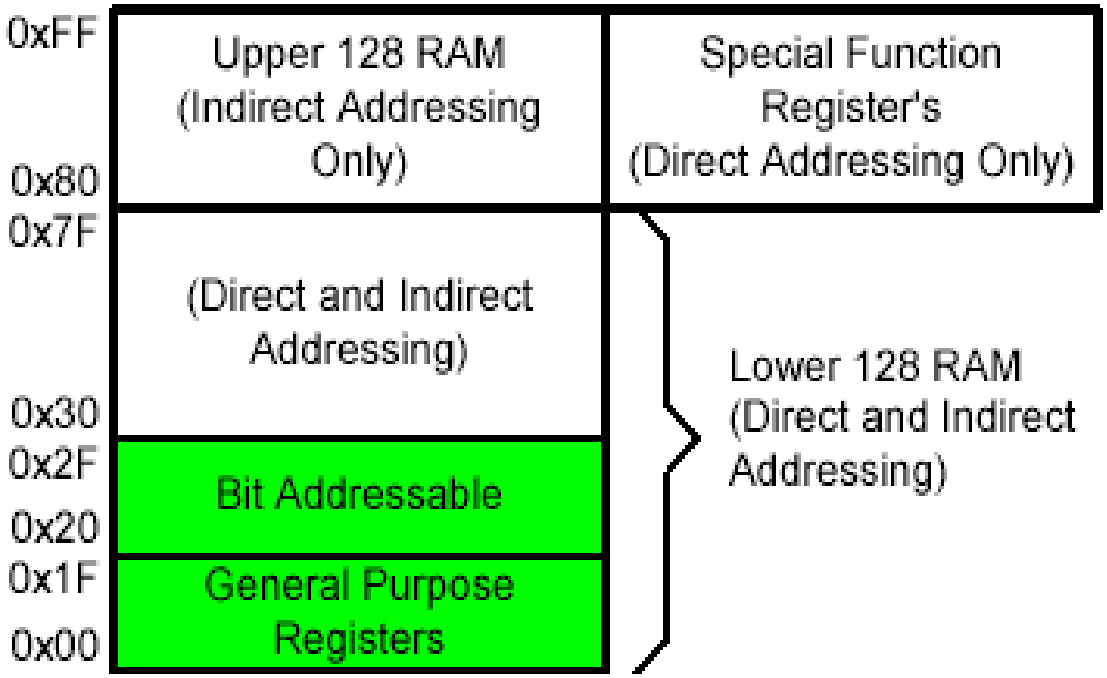
| CY | AC | F0 | RS1 | RS0 | OV | — | P |
|---|---|---|---|---|---|---|---|

| | | |
|---|---|---|
| CY | PSW.7 | Carry Flag. |
| AC | PSW.6 | Auxiliary Carry Flag. |
| F0 | PSW.5 | Flag 0 available to the user for general purpose. |
| RS1 | PSW.4 | Register Bank selector bit 1 (SEE NOTE 1). |
| RS0 | PSW.3 | Register Bank selector bit 0 (SEE NOTE 1). |
| OV | PSW.2 | Overflow Flag. |
| — | PSW.1 | User definable flag. |
| P | PSW.0 | Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of '1' bits in the accumulator. |

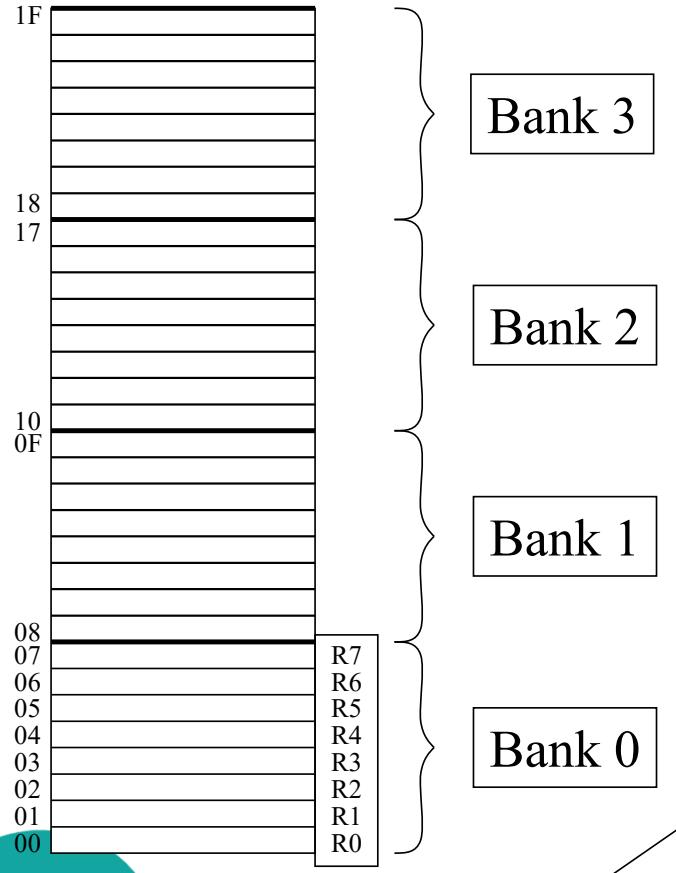
**NOTE:**
1. The value presented by RS0 and RS1 selects the corresponding register bank.

| RS1 | RS0 | Register Bank | Address |
|---|---|---|---|
| 0 | 0 | 0 | 00H-07H |
| 0 | 1 | 1 | 08H-0FH |
| 1 | 0 | 2 | 10H-17H |
| 1 | 1 | 3 | 18H-1FH |

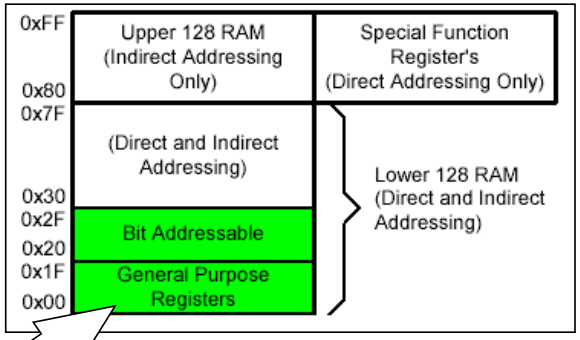
# On-Chip Memory
# Internal RAM



# Registers




Four Register Banks
Each bank has R0-R7
Selectable by psw.2,3



# Bit Addressable Memory

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 2F | 7F | | | | | | | 78 |
| 2E | | | | | | | | |
| 2D | | | | | | | | |
| 2C | | | | | | | | |
| 2B | | | | | | | | |
| 2A | | | | | | | | |
| 29 | | | | | | | | |
| 28 | | | | | | | | |
| 27 | | | | | | | | |
| 26 | | | | | | | | |
| 25 | | | | | | | | |
| 24 | | | | | | | | |
| 23 | | | | | | 1A | | |
| 22 | | | | | | | | 10 |
| 21 | 0F | | | | | | | 08 |
| 20 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |

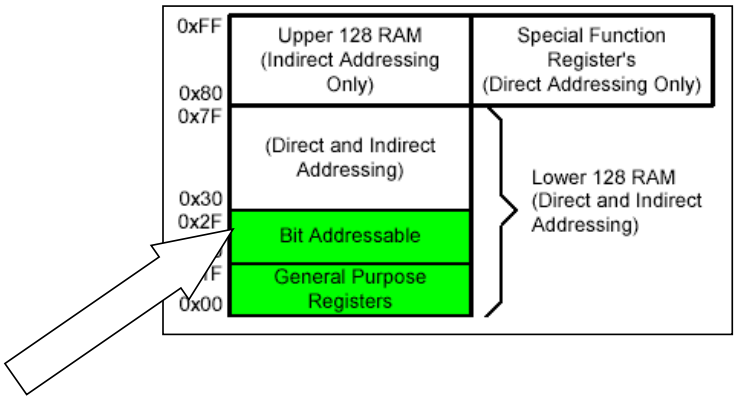
20h – 2Fh (16 locations X 8-bits = 128 bits)

Bit addressing:

mov C, 1Ah

or

mov C, 23h.2



# Bit Addressable RAM