SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)

Coimbatore-35

DEPARTMENT OF BIOMEDICAL ENGINEERING

I/O Ports

III Year/ VI Sem

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ASP / BME / SNSCT

IMPORTANT PINS (IO Ports)

- **One of the most useful features of the 8051 is that it contains four I/O ports (P0 - P3)**

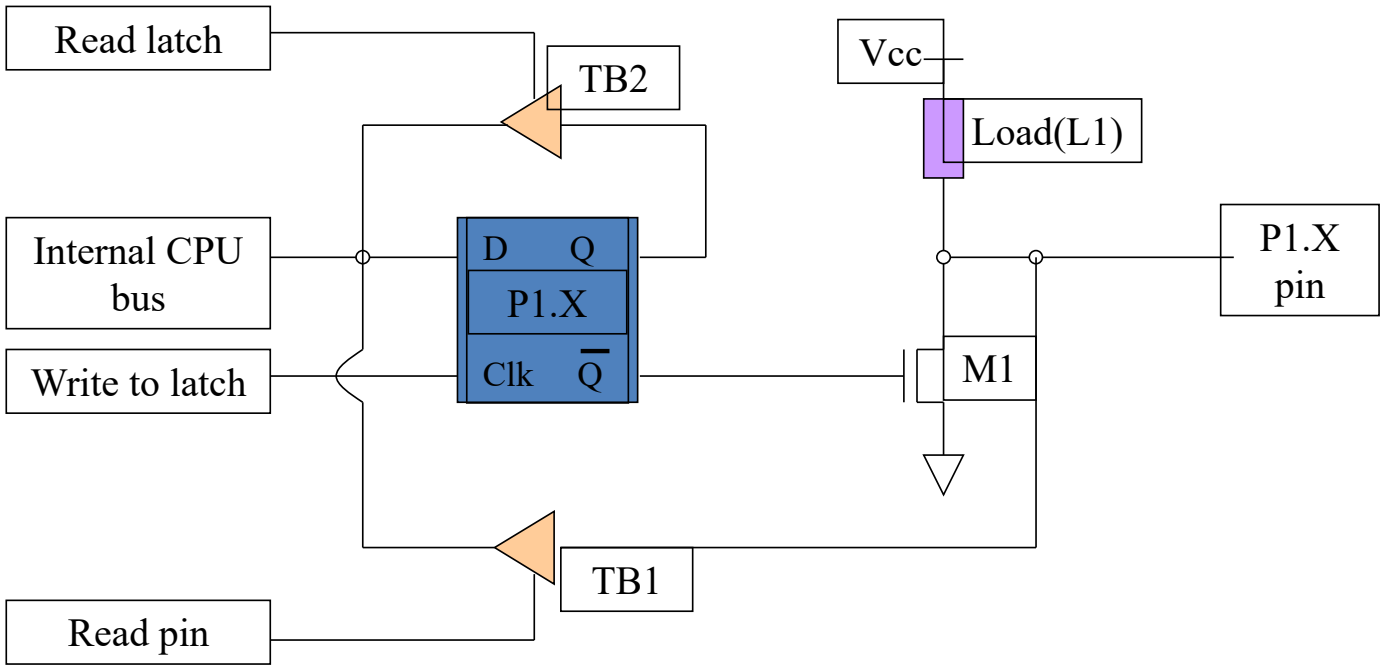
- Port 0 （pins 32-39）：P0（P0.0～P0.7）
  - 8-bit R/W - General Purpose I/O
  - Or acts as a multiplexed low byte address and data bus for external memory design

- Port 1 （pins 1-8） ：P1（P1.0～P1.7）
  - Only 8-bit R/W - General Purpose I/O

- Port 2 （pins 21-28）：P2（P2.0～P2.7）
  - 8-bit R/W - General Purpose I/O
  - Or high byte of the address bus for external memory design

- Port 3 （pins 10-17）：P3（P3.0～P3.7）
  - General Purpose I/O
  - if not using any of the internal peripherals (timers) or external interrupts.
- **Each port can be used as input or output (bi-direction)**

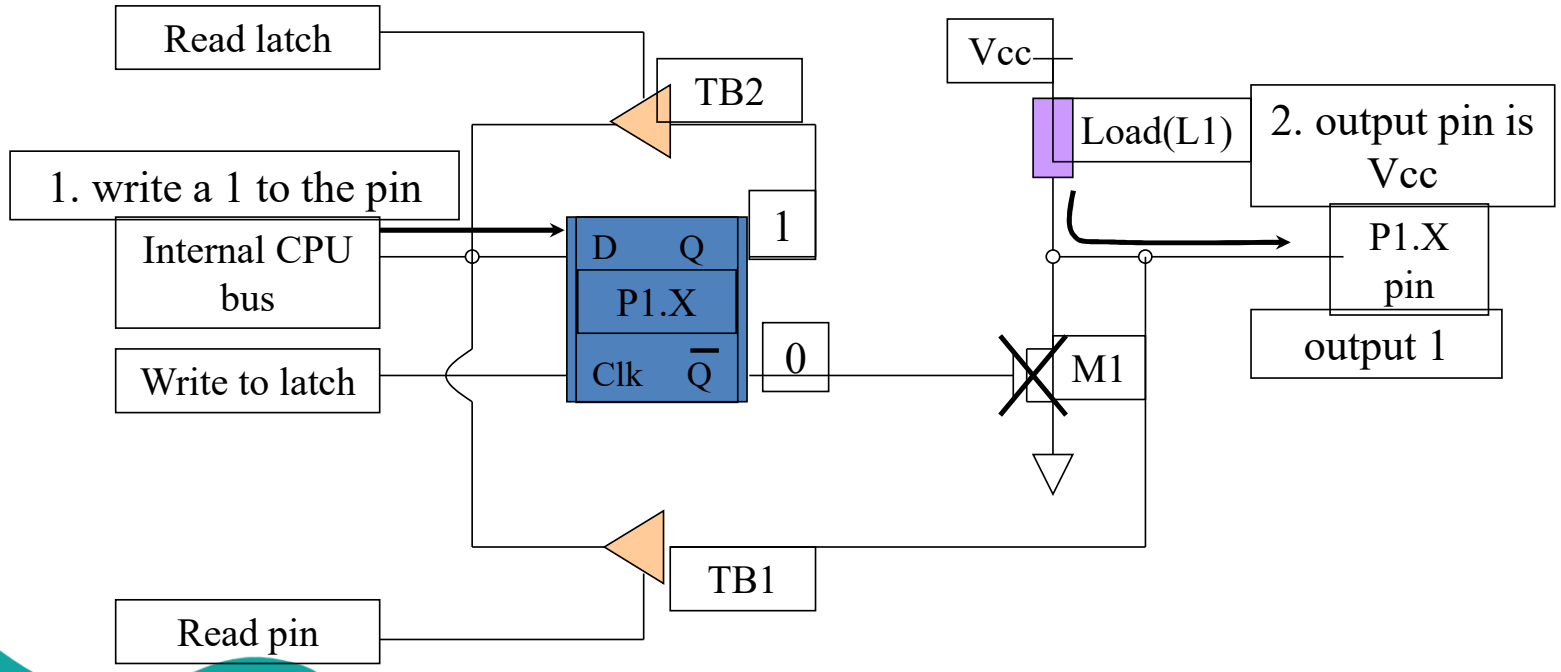
Hardware Structure of I/O Pin



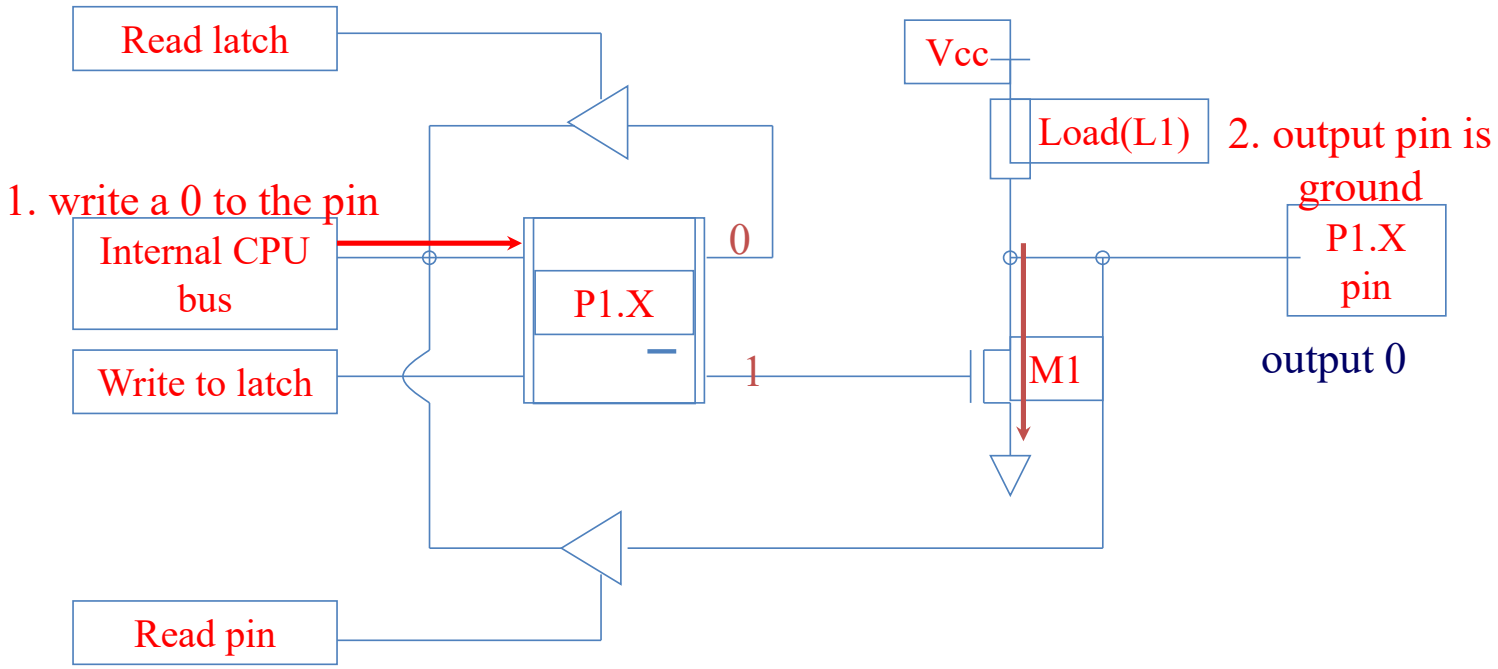
Hardware Structure of I/O Pin

- Each pin of I/O ports
  - Internally connected to CPU bus
  - A D latch store the value of this pin
    - Write to latch＝1：write data into the D latch
  - 2 Tri-state buffer：
    - TB1: controlled by “Read pin”
      - Read pin＝1：really read the data present at the pin
    - TB2: controlled by “Read latch”
      - Read latch＝1：read value from internal latch
  - A transistor M1 gate
    - Gate=0: open
    - Gate=1: close

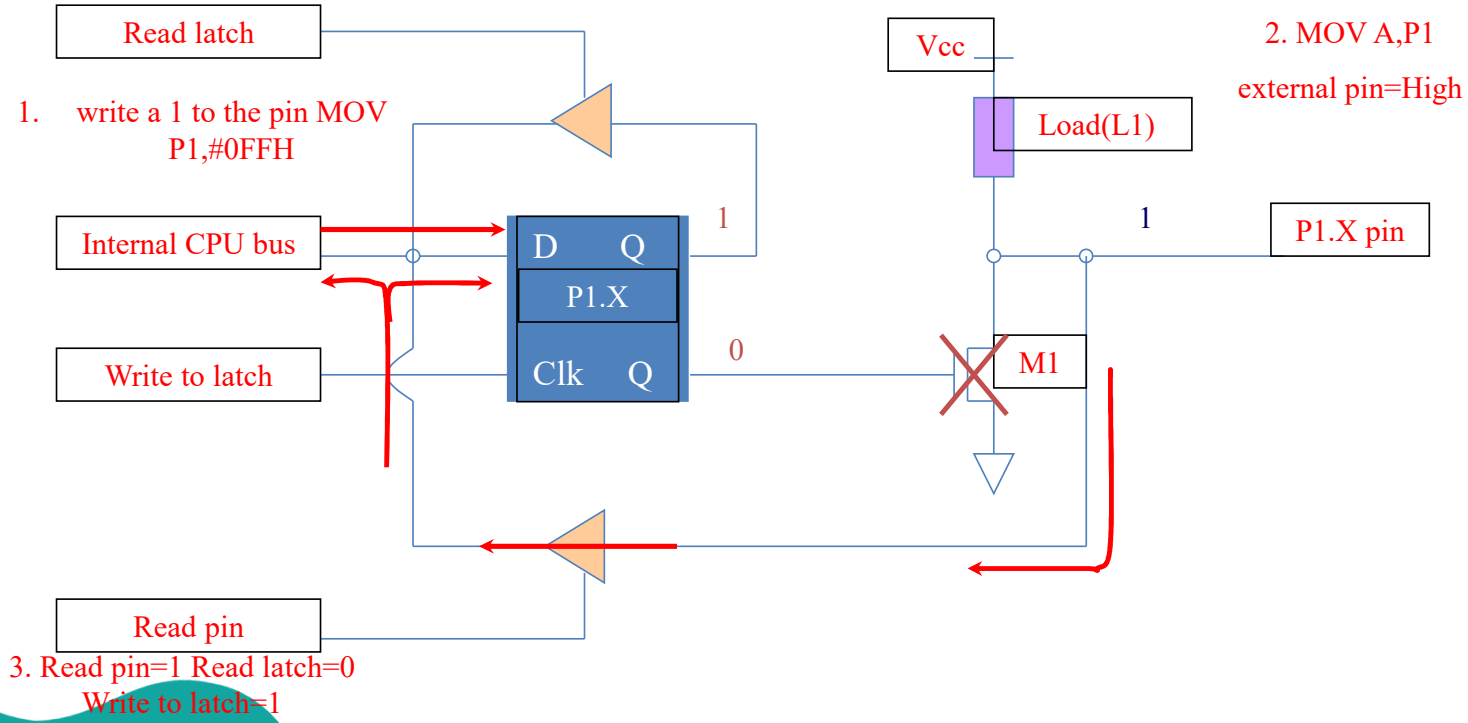
Writing "1" to Output Pin P1.X



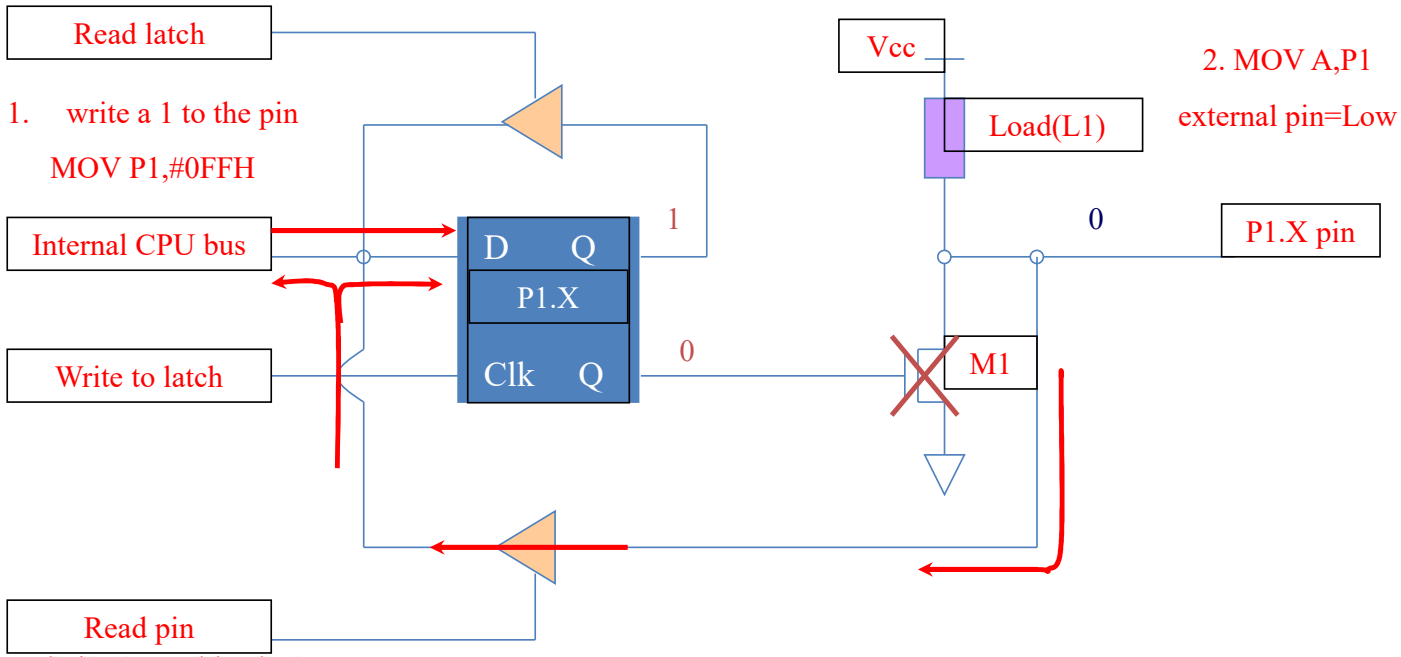
Writing "0" to Output Pin P1.X



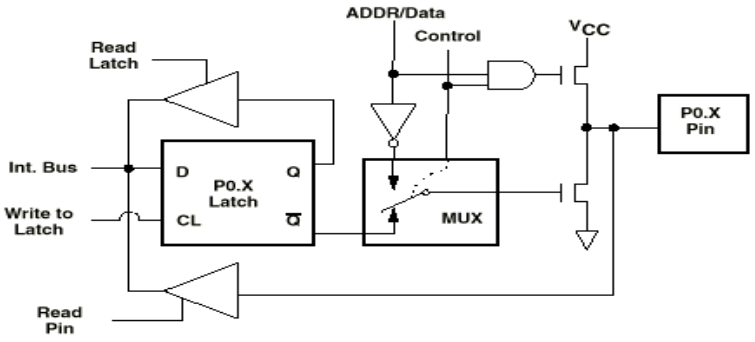
Reading "High" at Input Pin



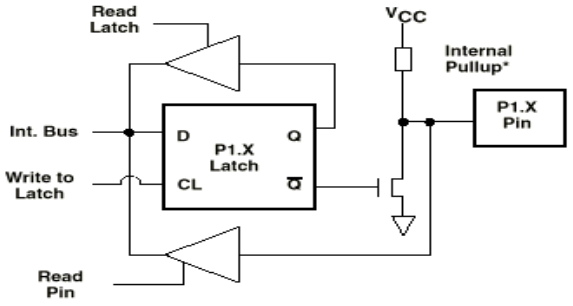
Reading "Low" at Input Pin



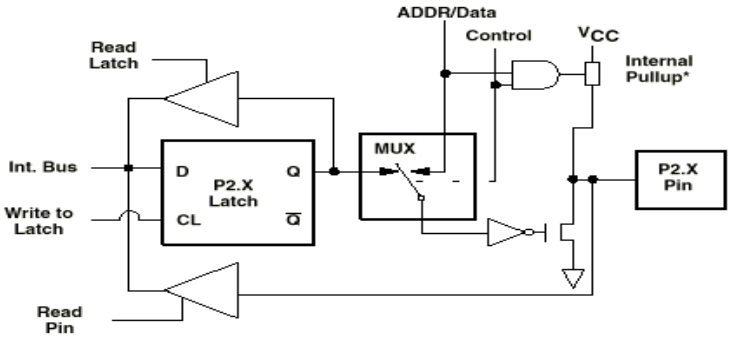
Ports



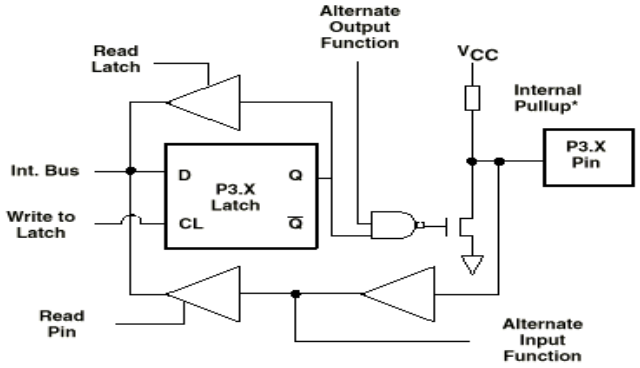
a. Port 0 Bit



b. Port 1 Bit

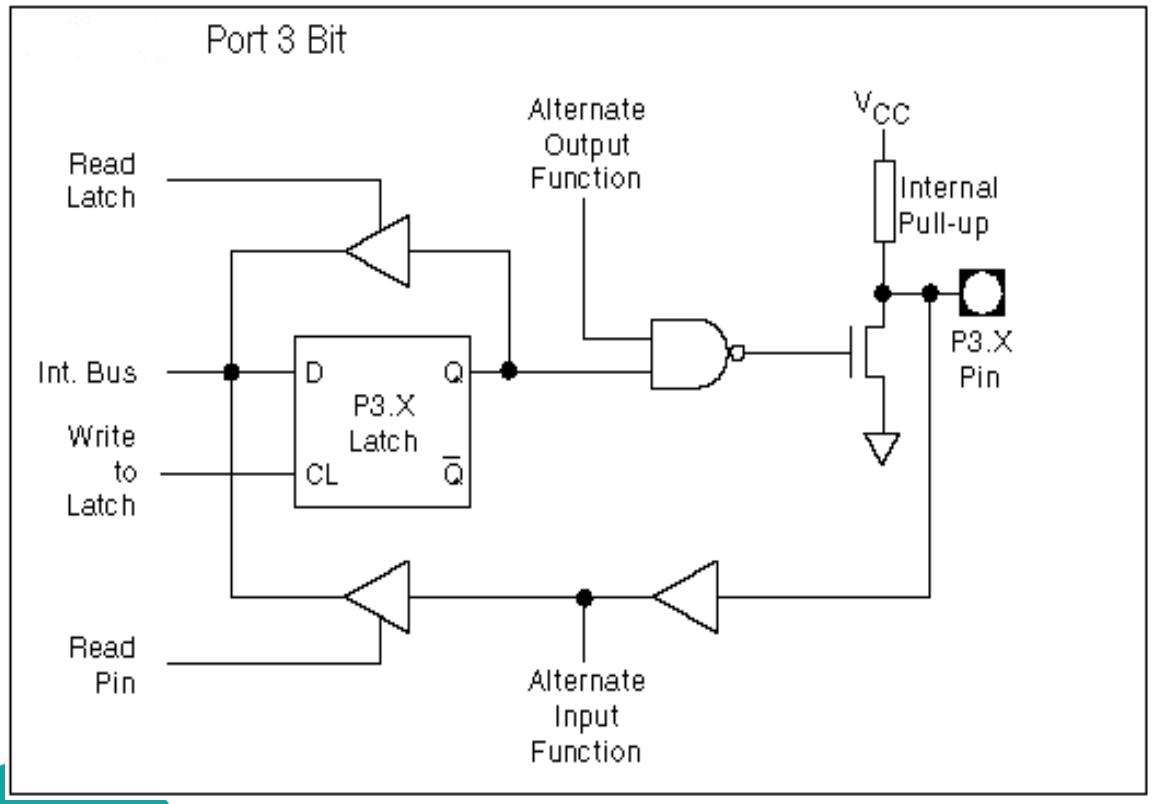


c. Port 2 Bit



d. Port 3 Bit

8051 Port 3 Bit Latches and I/O Buffers



Port 3 Alternate Functions

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)