



SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)

Coimbatore-35

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DEPARTMENT OF BIOMEDICAL ENGINEERING

Interrupt Process

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**Dr. K. Manoharan,
ASP / BME / SNSCT**



Interrupt Process

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If interrupt event occurs AND interrupt flag for that event is enabled, AND interrupts are enabled, then:

1. Current PC is pushed on stack.
2. Program execution continues at the interrupt vector address for that interrupt.
3. When a RETI instruction is encountered, the PC is popped from the stack and program execution resumes where it left off.



Interrupt Priorities

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- What if **two** interrupt sources interrupt at the **same time**?
- The interrupt with the highest PRIORITY gets serviced first.
- All interrupts have a default priority order.
- Priority can also be set to “high” or “low”.



Interrupt SFRs

Figure 12.9. IE: Interrupt Enable

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
EA	IEGF0	ET2	ES0	ET1	EX1	ET0	EX0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0xA8



Interrupt Vectors

Each interrupt has a **specific** place in **code** memory where program execution (interrupt service routine) begins.

External Interrupt 0:	0003h
Timer 0 overflow:	000Bh
External Interrupt 1:	0013h
Timer 1 overflow:	001Bh
Serial :	0023h
Timer 2 overflow (8052+)	002bh

Note: that there are only 8 memory locations between vectors.



Example Interrupt Service Routine



```
;EX7 ISR to blink the LED 5 times.  
;Modifies R0, R5-R7, bank 3.  
;-----
```

```
ISRBLK:    push PSW                ;save state of status word  
           mov PSW,#18h            ;select register bank 3  
           mov R0, #10             ;initialize counter  
Loop2:     mov R7, #02h            ;delay a while  
Loop1:     mov R6, #00h  
Loop0:     mov R5, #00h  
           djnz R5, $  
           djnz R6, Loop0  
           djnz R7, Loop1  
           cpl P1.6                ;complement LED value  
           djnz R0, Loop2          ;go on then off 10 times  
           pop PSW  
           reti
```