SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)

COIMBATORE-35

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

COURSE NAME: 19EEB303 / Microcontroller and its Applications

III YEAR / VI SEMESTER

Unit IV – ARM INSTRUCTION SET

Topic: Organization of CPU

ORGANIZATION OF CPU

The ARM CPU organization centers around a pipeline structure, typically a 3-stage (fetch, decode, execute) or 5-stage (fetch, decode, execute, buffer/data, write-back) process. It features a register bank, barrel shifter, ALU, and instruction decoder, all working together to efficiently execute instructions. The core components are designed for speed, with optimization for memory access and data manipulation.

ORGANIZATION OF CPU

A Advanced RISC Machine (ARM) Processor is considered to be the family of a Central Processing Units that are used in the music players, smartphones, wearables, tablets and the other consumer electronic devices. Advanced RISC Machines create a ARM processor architecture hence the name is ARM. This needs very few instruction sets and transistors. It is very small in size. This is the reason that it is a perfect fit for small-size devices.

It has less power consumption along with reduced complexity in its circuits. They can be applied to various designs such as 32-bit devices and embedded systems. They can even be upgraded according to user needs.

ORGANIZATION OF CPU

An ARM processor is a widely-used computer chip known for its efficiency and versatility. Designed by ARM Limited using a streamlined RISC architecture these processors are licensed to various companies rather than manufactured directly. ARM unique business model allows tech companies to customize and build processors for diverse devices, from smartphones and tablets to computers and smart devices. Their exceptional balance of processing power and energy efficiency has made them the preferred choice for mobile computing, enabling longer battery life without compromising performance.

FEATURES OF ARM PROCESSOR

Multiprocessing Systems

ARM processors are designed to be used in cases of multiprocessing systems where more than one processor is used to process information. The First AMP processor introduced by the name of ARMv6K could support 4 CPUs along with its hardware.

Tightly Coupled Memory

The memory of ARM processors is tightly coupled. This has a very fast response time. It has low latency (quick response) that can also be used in cases of cache memory being unpredictable.

Memory Management

ARM processor has a management section. This includes Memory Management Unit and Memory Protection Unit. These management systems become very important in managing memory efficiently.

FEATURES OF ARM PROCESSOR

Thumb-2 Technology

Thumb-2 Technology was introduced in 2003 and was used to create variable-length instruction sets. It extends the 16-bit instructions of initial Thumb technology to 32-bit instructions. It has better performance than previously used Thumb technology.

One-Cycle Execution Time

ARM processor is optimized for each instruction on the CPU. Each instruction is of a fixed length that allows time for fetching future instructions before executing the present instructions. ARM has CPI (Clock Per Instruction) of one cycle.

FEATURES OF ARM PROCESSOR

Pipelining

Processing of instructions is done in parallel using pipelines. Instructions are broken down and decoded in one pipeline stage. The channel advances one step at a time to increase throughput (rate of processing).

A large number of Registers

A large number of registers are used in ARM processors to prevent large amounts of memory interactions. Records contain data and addresses. These act as a local memory store for all operations.