SNS COLLEGE OF TECHNOLOGY

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

COURSE NAME: 19EEB303 / Microcontroller and its Applications

III YEAR / VI SEMESTER

Unit IV – ARM INSTRUCTION SET

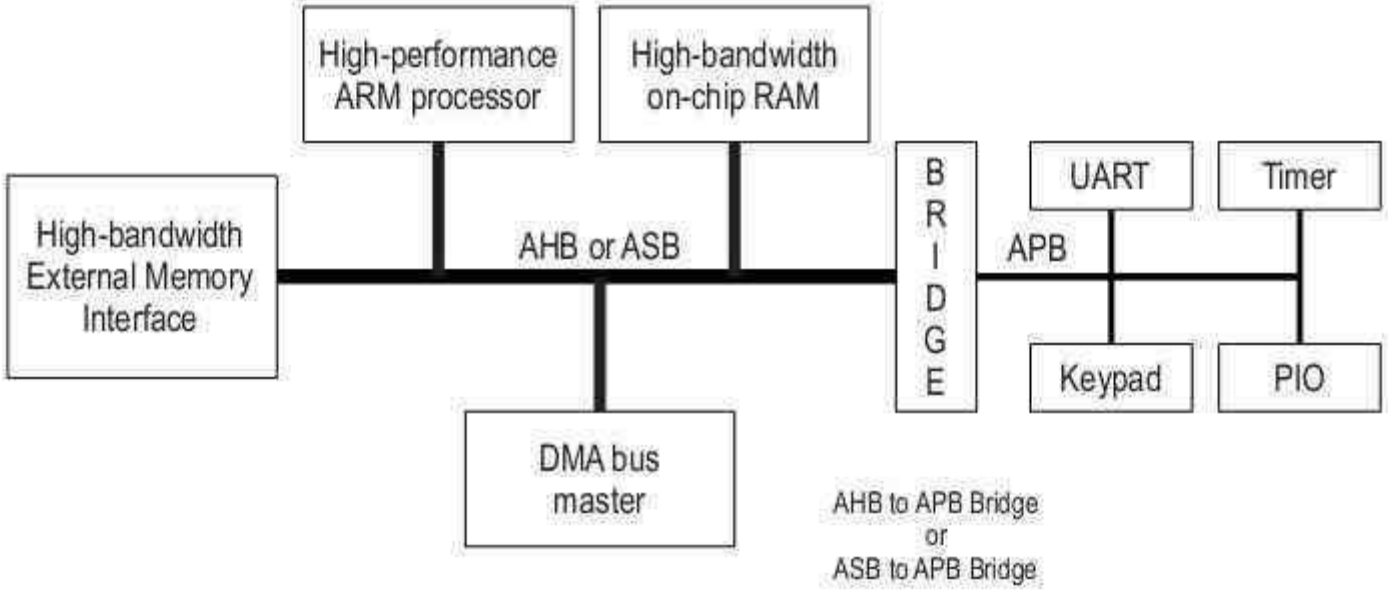
Topic: Bus Architecture

Bus Architecture

The AMBA specification defines an on-chip communication standard, used to design embedded microcontrollers with high performance. The ARM bus architecture typically utilizes the Advanced Microcontroller Bus Architecture (AMBA) standards, which include different bus protocols such as AHB (Advanced High-performance Bus), ASB (Advanced System Bus), and APB (Advanced Peripheral Bus). These protocols provide a structured and scalable communication framework for ARM-based systems.

Let us understand key components as shown in the ARM bus technology diagram. As shown, the ARM processor, high bandwidth memory, and on-chip RAM are connected via the high-performance AHB or AXI bus, ensuring rapid data access and processing. The DMA controller also uses this bus for efficient data transfers.

Bus Architecture



AMBA AHB

* High performance
* Pipelined operation
* Multiple bus masters
* Burst transfers

AMBA ASB

* High performance
* Pipelined operation
* Multiple bus masters

AMBA APB

* Low power
* Latched address and control
* Simple interface
* Suitable for many peripherals

Components of ARM Bus Architecture

- **ARM Processor:** The central processing unit (CPU) in the system, responsible for executing instructions and processing data. The ARM processor is usually connected to the high-performance AHB or AXI bus to ensure fast access to memory and other high-speed peripherals.
- **High Bandwidth Memory (HBM):** High-performance memory designed for high data throughput. It is typically connected to the ARM processor via the AHB or AXI bus to support rapid data access and transfer. HBM is essential for applications requiring large data bandwidth, such as graphics processing and machine learning.
- **High Bandwidth On-chip RAM:** On-chip RAM provides fast, low-latency storage for frequently accessed data. It is directly connected to the ARM processor through the high-speed AHB or AXI bus, ensuring quick data read/write operations essential for efficient processing.

Bus Architecture

- **DMA Bus Master:** Direct Memory Access (DMA) controller acts as a bus master, capable of transferring data between memory and peripherals without involving the CPU. This reduces CPU overhead and increases data transfer efficiency. The DMA controller is connected to the AHB or AXI bus for high-speed data movement.
- **Bus Bridges:** Bridges are used to connect different bus protocols within the system. For example, an AHB-to-APB bridge allows communication between high-speed AHB devices and lower speed APB peripherals. Bridges ensure seamless data transfer across different bus types.
- **AHB (Advanced High-performance Bus):** AHB is a high-speed, high-bandwidth bus designed for connecting high-performance components like CPUs, high-speed memory, and DMA controllers. It supports burst transfers and provides efficient data throughput for demanding applications.

Bus Architecture

- **ASB (Advanced System Bus):** ASB is an older, less common bus used for connecting system components. It provides a balance between performance and complexity, typically used in legacy designs.
- **APB (Advanced Peripheral Bus):** APB is a low-power, low-bandwidth bus designed for connecting peripheral devices like UARTs, timers, PIOs, and keypads. It simplifies the interface for these devices and reduces power consumption.
- **UART (Universal Asynchronous Receiver/Transmitter):** A peripheral device connected to the APB. UART is used for serial communication, enabling data exchange between the system and external devices. It is essential for debugging and communication in embedded systems.

Bus Architecture

•**Timer:** A peripheral connected to the APB. Timers are used for generating time delays, measuring time intervals, and triggering periodic events. They are critical for real-time applications and system scheduling.

•**PIO (Programmable Input/Output):** A peripheral connected to the APB. PIO provides configurable I/O pins that can be programmed to perform various input/output functions. Used for interfacing with external devices such as LEDs, switches, sensors and actuators. Each pin can be configured as an input or output and can often support various functions like interrupts or PWM.

•**Keypad:** A peripheral device connected to the APB. Keypads provide user input capabilities, typically used in embedded systems for user interface purposes. The APB connection ensures low power consumption and sufficient bandwidth for keypad scanning and input detection.