SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)

Coimbatore-35

DEPARTMENT OF BIOMEDICAL ENGINEERING

19BMB303 & Fundamentals of Microprocessors and Microcontrollers

Unit V - 32- BIT ARM PROCESSOR

III Year/ VI Sem

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ASP / BME / SNSCT

MICROCONTROLLER BASED SYSTEM DESIGN

Reduced Instruction Set Computer

Design Physiology

RISC Vs CISC Architecture

ARM Processor Architecture

ARM Core data flow model, Barrel Shifter

ARM processor modes and families

Pipelining

ARM instruction Set and its Programming

Pulse oximeter using ARM processor

ARM Processor Architecture

- In ARM controller RISC, load-store architecture exists in this board.
- Different types of registers are used in this board which helps in the manipulation of memory.
- The set of instructions is used in the board but the main function is to decrease the time required by every instruction.
- The processor used in the ARM controller is cortex M3 which is a high-speed and thirty-two-bit, and it offers numerous features to the users.
- The architecture of this board is Harward architecture has distinct data and instruction buses to transmit data to the random access memory and read-only memory unknit.

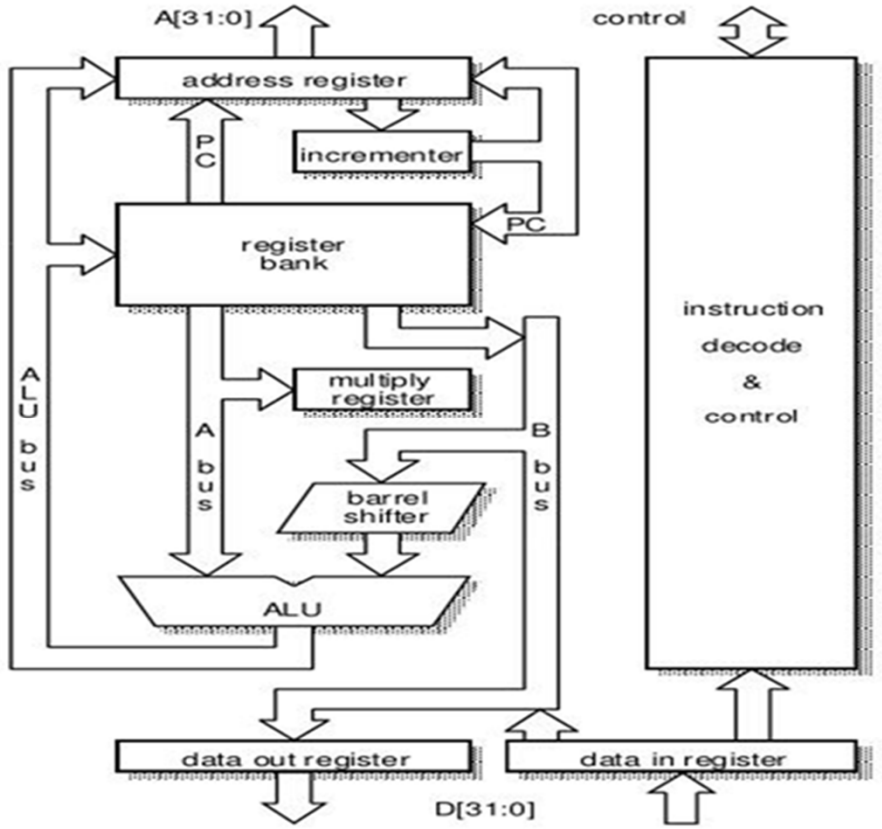
ARM Processor Architecture

- For execution, fetching, decoding, and different types of commands three-stage pipeline is used.
- The processor of this board uses thumb commands based on the thumb two techniques, so it decreases the memory needed for the program and makes sure of a higher density of coding.
- This model comprises a thirty-two-bit architecture which provides better performance in the execution of commands.

ARM Processor Architecture

Key Features of ARM7TDMI:

- **32-bit RISC Architecture** (Reduced Instruction Set Computer)
- **Von Neumann Architecture** (shared instruction and data bus)
- **3-stage Pipeline**: Fetch, Decode, Execute
- **TDMI stands for**:
  - **T** – Thumb instruction set support (16-bit compressed instructions)
  - **D** – Debug support (JTAG)
  - **M** – Multiplier (enhanced 32 × 32-bit multiplier)
  - **I** – In-circuit emulator (ICE) support



ARM Processor Architecture

1. Register File:

- 16 general-purpose registers (R0–R15)
- R13 = Stack Pointer (SP)
- R14 = Link Register (LR)
- R15 = Program Counter (PC)
- CPSR (Current Program Status Register) and SPSR (Saved PSR for exceptions)

2. ALU (Arithmetic Logic Unit):

- Performs integer arithmetic and logic operations

3. Barrel Shifter:

- Efficient shifting and rotating of operands (before ALU operations)

ARM Processor Architecture

4. Multiplier:

- 32×32 multiplier for fast multiplication operations

5. Instruction Decoder:

- Decodes both ARM (32-bit) and Thumb (16-bit) instructions

6. Pipeline:

- **3 stages**:
  - **Fetch**: Gets instruction from memory
  - **Decode**: Decodes instruction and prepares operands
  - **Execute**: Executes instruction, memory access or register write-back

7. Bus Interface:

- Connects CPU to memory and peripherals via AHB, AMBA, or custom buses

ARM Processor Architecture

Program Status Registers:

- **CPSR** – Current Program Status Register (flags, mode bits)
- **SPSR** – Saved Program Status Register (used in exception handling)

Instruction Decoder

- **Handles decoding of ARM (32-bit) and Thumb (16-bit) instructions**

Mode	Instruction Size	Description
ARM	32-bit	Full instruction set, more powerful
Thumb	16-bit	Compressed instructions, saves memory, slower but compact