SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)

Coimbatore-35

DEPARTMENT OF BIOMEDICAL ENGINEERING

19BMB303 & Fundamentals of Microprocessors and Microcontrollers

Unit V - 32- BIT ARM PROCESSOR

III Year/ VI Sem

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ASP / BME / SNSCT

MICROCONTROLLER BASED SYSTEM DESIGN

Reduced Instruction Set Computer

Design Physiology

RISC Vs CISC Architecture

ARM Processor Architecture

ARM Core data flow model, Barrel Shifter

ARM processor modes and families

Pipelining

ARM instruction Set and its Programming

Pulse oximeter using ARM processor

Instruction Set

Category	Description
Data Processing	Arithmetic and logical operations
Data Transfer	Load and store (memory access)
Control Flow	Branching and subroutine calls
Program Status Access	Access or modify status/control registers
Co-processor	Communication with co-processors
Software Interrupt	Generates a software-triggered exception

Data Processing Instructions

Instruction	Operation	Syntax	Example	Description
ADD	Addition	ADD Rd, Rn, Operand2	ADD R0, R1, R2	R0 = R1 + R2
SUB	Subtraction	SUB Rd, Rn, Operand2	SUB R4, R5, #10	R4 = R5 - 10
RSB	Reverse Subtract	RSB Rd, Rn, Operand2	RSB R6, R7, #100	R6 = 100 - R7
ADC	Add with Carry	ADC Rd, Rn, Operand2	ADC R1, R2, R3	R1 = R2 + R3 + Carry
SBC	Subtract with Carry	SBC Rd, Rn, Operand2	SBC R4, R5, R6	R4 = R5 - R6 - (1 - Carry)

Data Processing Instructions

Instruction	Operation	Syntax	Example	Description
MOV	Move	MOV Rd, Operand2	MOV R0, #0xFF	R0 = 0xFF
MVN	Move NOT (bitwise NOT)	MVN Rd, Operand2	MVN R7, #0	R7 = 0xFFFFFFFF
AND	Bitwise AND	AND Rd, Rn, Operand2	AND R0, R1, R2	R0 = R1 AND R2
ORR	Bitwise OR	ORR Rd, Rn, Operand2	ORR R3, R3, #0x01	Set lowest bit in R3
EOR	Exclusive OR	EOR Rd, Rn, Operand2	EOR R4, R5, R6	R4 = R5 XOR R6

Data Processing Instructions

Instruction	Operation	Syntax	Example	Description
BIC	Bit Clear	BIC Rd, Rn, Operand2	BIC R0, R1, #0xF	Clears specified bits in R1 and stores in R0
CMP	Compare (no result)	CMP Rn, Operand2	CMP R1, R2	Updates flags as if R1 - R2
CMN	Compare Negative	CMN Rn, Operand2	CMN R3, #5	Updates flags as if R3 + 5
TST	Test bits (AND)	TST Rn, Operand2	TST R4, #0x01	Updates flags from R4 AND 0x01
TEQ	Test Equivalence (XOR)	TEQ Rn, Operand2	TEQ R5, #0x0F	Updates flags from R5 XOR 0x0F

Data Transfer Instructions

Instruction	Operation	Syntax	Example	Description
LDR	Load Register	LDR Rd, [Rn, #offset]	LDR R0, [R1, #4]	Load word from address (R1 + 4) into R0
STR	Store Register	STR Rd, [Rn, #offset]	STR R2, [R3, #8]	Store word from R2 into memory at (R3 + 8)
LDRB	Load Register Byte	LDRB Rd, [Rn, #offset]	LDRB R4, [R5]	Load 8-bit byte from address in R5 into R4
STRB	Store Register Byte	STRB Rd, [Rn, #offset]	STRB R6, [R7, #1]	Store 8-bit byte from R6 into memory (R7 + 1)
LDRH	Load Halfword (16 bits)	LDRH Rd, [Rn, #offset]	LDRH R8, [R9]	Load 16-bit halfword from memory into R8
STRH	Store Halfword	STRH Rd, [Rn, #offset]	STRH R10, [R11]	Store 16-bit halfword from R10 into memory

Data Transfer Instructions

Instruction	Operation	Syntax	Example	Description
LDM	Load Multiple	LDM Rn!, {Rlist}	LDM R0!, {R1-R3}	Load multiple registers from memory
STM	Store Multiple	STM Rn!, {Rlist}	STM R4!, {R5-R7}	Store multiple registers into memory
LDR (Label)	Load from address label	LDR Rd, =label	LDR R0, =myData	Load address of label into R0
STR (Label)	Store to label address	STR Rd, =label (via pointer)	STR R1, [R2] with R2 = myData	Store R1 into memory pointed to by label address

Control Flow Instructions

Instruction	Operation	Syntax	Example	Description
B	Branch (Unconditional)	B label	B loop_start	Jumps to the label loop_start
BL	Branch with Link	BL label	BL function_call	Calls subroutine and saves return address in LR (R14)
BX	Branch and Exchange	BX Rn	BX LR	Returns from subroutine using address in LR
BEQ	Branch if Equal	BEQ label	BEQ done	Branches to done if Zero flag (Z) is set
BNE	Branch if Not Equal	BNE label	BNE retry	Branches if Zero flag (Z) is clear (not equal)
BGT	Branch if Greater Than	BGT label	BGT positive_result	Branches if result is greater than zero (signed)

Control Flow Instructions

Instruction	Operation	Syntax	Example	Description
BLT	Branch if Less Than	BLT label	BLT negative_result	Branches if result is less than zero (signed)
BGE	Branch if Greater or Equal	BGE label	BGE finish	Branches if greater than or equal (signed)
BLE	Branch if Less or Equal	BLE label	BLE check_next	Branches if less than or equal (signed)
BHI	Branch if Higher	BHI label	BHI overflow_case	Branches if unsigned higher (C=1 and Z=0)
BLS	Branch if Lower or Same	BLS label	BLS fail_case	Branches if unsigned lower or same (C=0 or Z=1)
SWI	Software Interrupt	SWI #number	SWI 0x11	Invokes software interrupt — used for OS/syscalls (e.g., I/O)

Program Status Access

Instruction	Operation	Syntax	Example	Description
MRS	Move from PSR to Register	MRS Rd, CPSR / MRS Rd, SPSR	MRS R0, CPSR	Reads current/saved program status register into a general-purpose register
MSR	Move to PSR from Register	MSR CPSR_f, Rn	MSR CPSR_f, R1	Writes value from register R1 to the flags field of CPSR
MSR	Move to PSR from Immediate	MSR CPSR_c, #value	MSR CPSR_c, #0x1F	Sets mode bits in CPSR (e.g., switch to user/system mode)

Program Status Access

Instruction	Operation	Syntax	Example	Description
MSR	Update specific PSR fields	MSR CPSR_fsxc, Rn	MSR CPSR_c, #0x80	Updates selected fields (flags, status, control) using field specifiers
MRS	Read SPSR (in exception modes)	MRS Rd, SPSR	MRS R3, SPSR	Reads the saved program status register (only in privileged modes)
MSR	Write SPSR	MSR SPSR_cxsf, Rn	MSR SPSR_fsxc, R2	Writes to the SPSR (used during exception handling or context switching)