SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)

COIMBATORE-35

Accredited by NBA-AICTE and Accredited by NAAC – UGC with A++ Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

COURSE NAME: 19EEB303 / Microcontroller and its Applications

III YEAR / VI SEMESTER

Unit IV – ARM INSTRUCTION SET

Topic: Addressing Modes of ARM

Addressing Modes of ARM

Addressing modes in ARM

To access memory, load and store instructions are utilised, as previously mentioned. The various memory access addressing modes are as follows:

(i) Register indirect addressing mode
(ii) Indirect addressing mode for relative registers
(iii) Indirect addressing method with a base index
(iv) Scale register addressing mode as a base

Addressing Modes of ARM

Register indirect addressing mode

- A register is utilised in this addressing mechanism to provide the address of the memory region to be accessed.
- **LDR R0, [R1] is an example**.
- This instruction loads the 32-bit word at the memory location contained in register R0 into register R0. This is known as Register indirect addressing mode.

Addressing Modes of ARM

Indirect addressing mode for relative registers

An instantaneous value applied to a register generates the memory address in this addressing style. This method of Addressing modes in ARM allows for both pre- and post-indexing.

For example, (a) LDR R0, [R1, #4]

This instruction loads the register R0 with the word at the memory regions computed by adding the constant address included in the R1 register value 4 to the memory address stored in the R1 register, e.g. (b) LDR R0, [R1, #4]!

Addressing Modes of ARM

Indirect addressing method with a base index

In this Addressing modes in ARM , The memory address is produced by adding the values of two registers in this addressing scheme.

For example, (a) LDR R0, [R1, R2]

Pre indexing and post indexing is also supported.

This instruction will load the word at the memory address determined by adding register R1 and register R2 into register R0.

For example, (b) LDR R0, [R1, R2]!

This is pre-index addressing.

This instruction loads the word at the memory location supplied in register R1 into register R0. The new address will then be calculated by adding the value in register R2 to register R1 and placed in R1.

Addressing Modes of ARM

Scaled register addressing mode as a base

In this Addressing modes in ARM, the memory address is produced by adding a register value to another register that is moved left in this addressing scheme. This addressing technique allows for pre-indexing and post-indexing.

For eg., (a) LDR R0, [R1, R2, LSL #2]

The word at the memory location computed by adding register R1 and register R2 shifted left by 2 bits will be loaded into register R0 using this command. For instance, (b) LDR RO,[R1, R2, LSL #2]!