SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB302–VLSI DESIGN

III YEAR/ V SEMESTER

UNIT 1 –MOS TRANSISTOR PRINCIPLE

TOPIC 7 –CV CHARACTERISTICS

MOS C-V CHARACTERISTICS

❖ The measured MOS capacitance (called gate capacitance) varies

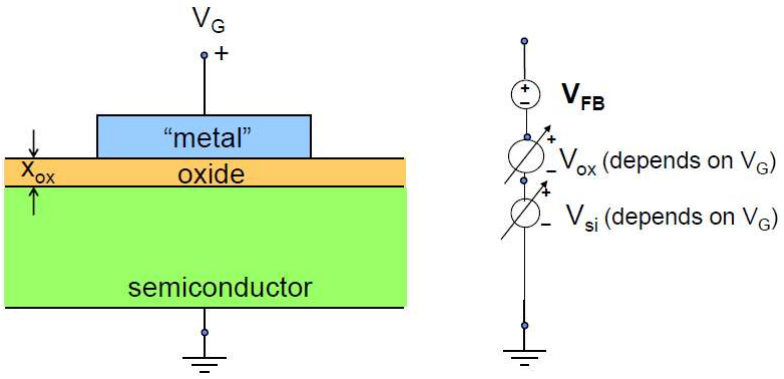
with the applied gate voltage

- A very powerful diagnostic tool for identifying any deviations from the ideal in both oxide and semiconductor
- Routinely monitored during MOS device fabrication

MEASUREMENT OF C-V CHARACTERISTICS

- Measurement of C-V characteristics
  - Apply any dc bias, and superimpose a small ac signal
  - Generally measured at 1 MHz (high frequency) or at variable frequencies between 1KHz to 1 MHz
  - The dc bias *V*G is slowly varied to get **quasi-continuous** C-V characteristics

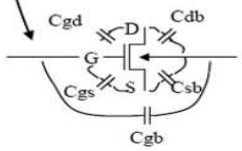
THE MOS CAPACITOR



$$V_G = V_{FB} + V_{ox} + V_{Si}$$

THE MOS CAPACITOR

- Three main forms:
  - Gate capacitance (gate of transistor)
  - Diffusion capacitance (drain regions)
  - Routing capacitance (metal, etc.)



Cg = Cgb + Cgs + Cgd
Approximated by
C = CoxA
Cox = thin oxide cap
A = area of gate

VFB: Flat Band Voltage (depends on semiconductor work function)

Vox = voltage drop across oxide (depends on VG)

VSi = voltage drop in the silicon (depends on VG)

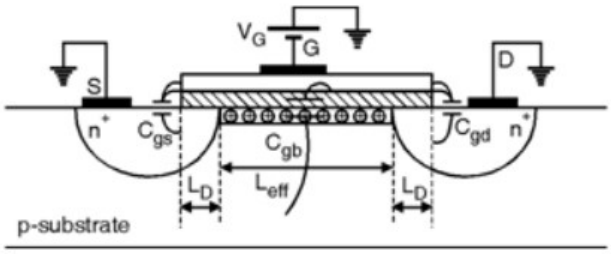
$$V_G = V_{FB} + V_{ox} + V_{Si}$$

CAPACITANCE OF MOS DEVICE IN ACCUMALATION

- The small signal capacitance is defined as $C = \frac{dQ}{dV}$
- First, consider a MOS device in accumulation
- Under sufficiently high voltage, accumulation layer thickness is very small.
- The separation between the metal and semiconductor charge approaches the oxide thickness.
- Consequently the capacitance approaches the oxide capacitance,

$C = C_{ox} = \varepsilon_{ox}/x_{ox}$: accumulation

CAPACITANCE OF MOS DEVICE IN ACCUMALATION



There are three types of capacitances are involved that are
1.Capacitance between gate electrode and substrate (C_{gb}),
2.Capacitance between gate and drain terminals (C_{gd})
3. Capacitance between gate and source terminals (C_{gs})

CAPACITANCE OF MOS DEVICE IN DEPLETION

- At flat band voltage, $V_G = V_{FB}$, the accumulation layer disappears
  - and the capacitance decreases.
- As V_G is increased beyond V_{FB}, MOS is biased into depletion.
  - The semiconductor surface region is depleted and
  - the total capacitance is composed of the oxide capacitance and the depletion layer capacitance.

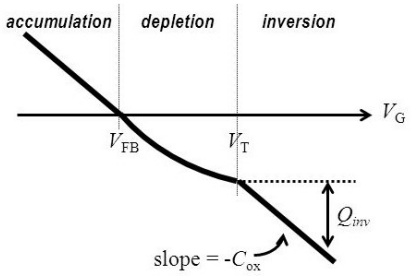
$$C = \left(\frac{1}{C_{ox}} + \frac{1}{C_s} \right)^{-1}$$

CAPACITANCE OF MOS DEVICE IN INVERSION

- Inversion layer charge responds to the measuring voltage.
- Since inversion layer is very thin in strong inversion,

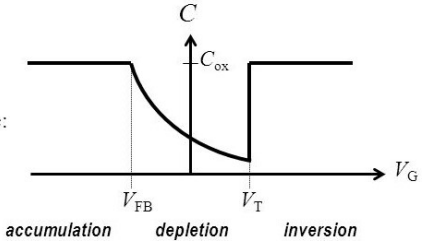
$$C = C_{ox} = \frac{\varepsilon_{ox}}{x_{ox}}$$

CV CHARACTERISTICS

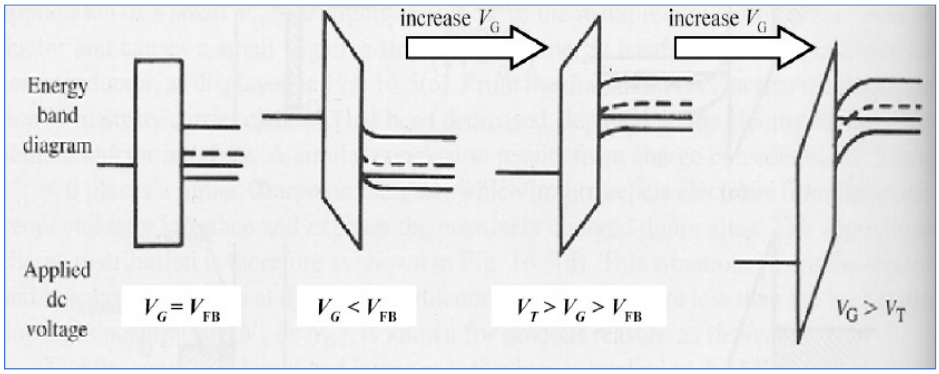


$$C = \left| \frac{dQ_s}{dV_G} \right|$$

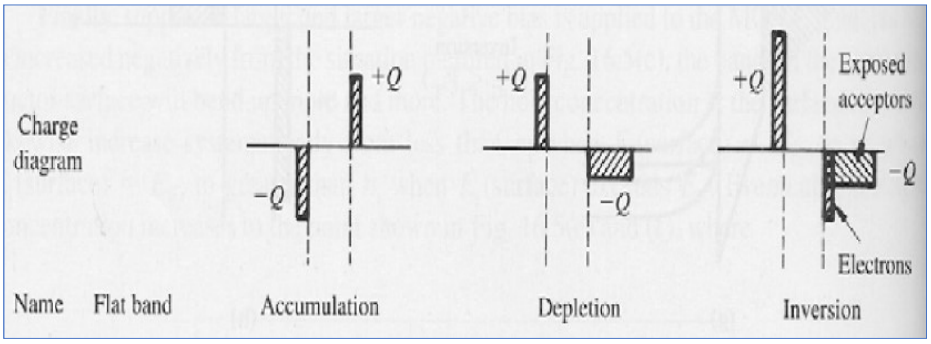
Ideal C-V curve:



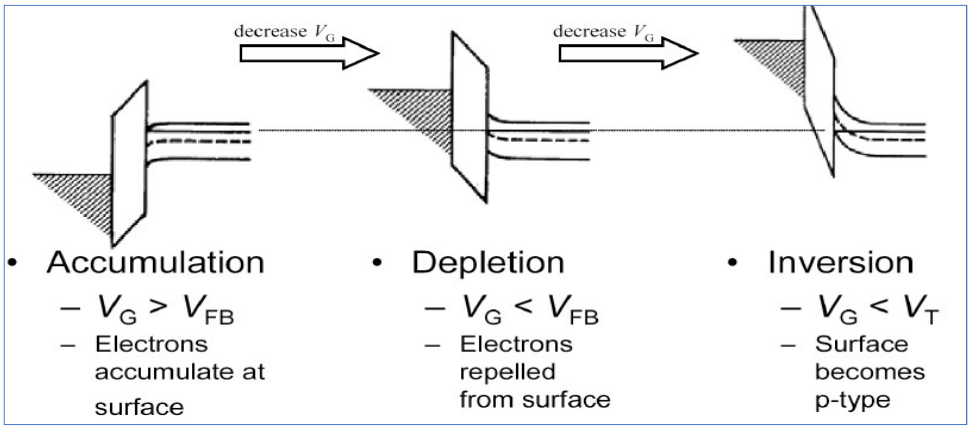
ENERGY BAND DIAGRAM



CHARGE DIAGRAM



MOS BAND DIAGRAM



- Accumulation
  - $V_G > V_{FB}$
  - Electrons accumulate at surface
- Depletion
  - $V_G < V_{FB}$
  - Electrons repelled from surface
- Inversion
  - $V_G < V_T$
  - Surface becomes p-type

ASSESSMENT

1. **Mode of operation**
2. **Region of operation**
3. **Capacitance in MOSFET**

THANK YOU