B.E (FT) END SEMESTER ARREAR EXAMINATIONS – NOV / DEC 2023

Computer Science and Engineering

Fourth Semester

CS6107 – COMPUTER ARCHITECTURE

(Regulation 2018 - RUSA)

Time: 3 Hours | Answer ALL Questions | Max. Marks 100

Note: Assume data, if required

PART-A (10 x 2 = 20 Marks)

1.	Specify the instruction format for R type instruction, give example.	2
2.	What are condition codes? How are they used?	2
3.	Illustrate how jump address is computed.	2
4.	Discuss the following instruction of MIPS: beq, addi	2
5.	Design a 8 bit adder using full adders.	2
6.	Apply bit pair recoding on the multiplier 100001110.	2
7.	State the principle behind loop unrolling.	2
8.	Discuss the concept of (m,n) predictorwith an example.	2
9.	How do we accomplish memory interleaving?	2
10.	DMA results in cycle stealing? Why is it called so?	2

PART – B (8 x 8 = 64 marks)

(Answer any 8 questions)

11.	State the processor performance equation I. Discuss in detail the influence of various parameters and derive performance equation II.	8
12.	Write a MIPS assembly language program to find the total ofthe given five marks stored in an array.	8
13.	Explain how subroutines are handled in MIPS architecture. Illustrate with a subroutine to find the given number is prime.	8
14.	Summarize the different addressing modes used in MIPS architecture and explain the address computation with example.	8
15.	State and explain Booth's algorithm. Simulate Booth's algorithm to find -5*6.	8

16.	Illustrate the division algorithm with a sequential circuit and flowchart. Simulate it for 11/3	8
17.	Explain the working of floating point addition with a circuit and flowchart.	8
18.	Draw the data path for lw $s0, 4($s1) and explain.	8
19.	Explain the control signals generated byALU control unit and also tabulate the description for the possible states of the control signals	8
20.	Elaborate the different cache mapping techniques. Illustrate the mapping techniques with suitable examples. Draw the implementation of 2-way set-associative cache with a cache of size 1K blocks.	8
21.	Explain the concept of virtual memory. Explain how address translation is made faster using TLB.	8
22.	Describe the working of I/O transfer where processor is relieved with neat illustration.	8
	PART – C (2 x 8 = 16marks)	
23.	Discuss in detail the dynamic branch prediction strategies with necessary illustrations.	8

24.	Identify the dependencies and hazards in the following code sequence. Also suggest solutions for the hazards identified.
	LD R1, 0(R3)
	SUB R4, R1, R3
	LD R4, 32(R5)
	ADD R1, R1, R4
	SUB R3, R4, R2
	LD R4, 32(R3)
	SD R4, 50(R1)
		8

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 30948

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Fifth Semester

Electronics and Communication Engineering

EC 2303 — COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to Sixth Semester Biomedical Engineering)

(Regulation 2008)

(Also common to PTEC 2303 – Computer Architecture and Organization for B.E. (Part-Time) Fourth Semester – Electronics and Communication Engineering – Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Write any two types of instruction.

2. Let X = 1010100 and Y = 1000011. Perform

   (a) X-Y and

   (b) Y-X using 2's complement.

3. How overflow is detected in fixed point arithmetic?

4. What is the difference between restoring and non-restoring division algorithms?

5. Define superscalar processing.

6. What is meant by Nano programming?

7. What are the advantages of RISC processor?

8. What is bus arbitration?

9. Differentiate RISC and CISC processors.

10. What are vector interrupts ?

PART B — (5 × 16 = 80 marks)

11. (a) Explain the various addressing modes in detail.

Or

(b) (i) With suitable example explain fixed point and floating point number representation in computers. (10)

(ii) Write notes on evolution of computers. (6)

12. (a) Explain 8 bit booth multiplier using flowchart and find the result to multiply $(-22) \times (44)$.

Or

(b) Explain the algorithm for floating point addition with a flowchart.

13. (a) Explain the hardwired and micro programmed control systems. (16)

Or

(b) Explain instruction pipelining with an example. (16)

14. (a) (i) Explain in detail about the replacement policies of memory organization systems. (8)

(ii) Give the structure of semiconductor RAM memories. Explain the read and write operations in details. (8)

Or

(b) Explain in detail about the cache memory organization cache operation and address mapping. (16)

15. (a) Stacks and subroutines need passing parameters through registers. Justify this statement using suitable calling program and subroutine. How I/O operations display few characters or line of characters. What are the various formats for it?

Or

(b) How the different generations evolved paving way to the present generation? What are the features of RISC and CISC processors? How do Dual and Quad processing evolved?

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Question Paper Code : X 10367

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
Fifth Semester
Electronics and Communication Engineering
EC 8552 – COMPUTER ARCHITECTURE AND ORGANIZATION
(Common to Electronics and Telecommunication Engineering)
(Regulations 2017)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. What is the impact of frequency of clock signal applied to the microprocessor in the performance of computers ?

2. Identify the addressing mode involved in the instruction XOR R1, [R2 + 100], R1 and determine the resultant stored in register R1 if all of its bit were 1's initially. (Assume three address instruction format in which the first two operands are source and the last one is the destination)

3. Draw the circuit schematic of a bit-cell using primitive gates that implements carry generate and propagate signals along with the sum bit of a pairwise inputs and carry signal from the preceding stage.

4. What is the meaning of biased exponent ? State the values of bias in the IEEE 754-1985 single and double precision formats, respectively.

5. State the purpose of the following registers in processor architectures : PC, MDR, IR and MAR.

6. State whether the instruction sequence MUL R3, R1, R2 and SUB R2, R3, R1 in succession when executed using a four stage pipelined processor will result in hazard or not. Justify.

7. What is the purpose of tag field in addressing a cache memory ? Assuming that processor generates 16 bit address and that the cache memory is organized as a 64 blocks of 16 words in every block, estimate the number of bits required for the tag field.

8. What is baud rate ? Is this term associated with serial or parallel communication standard ?

9. What are the types of hardware multithreading ? How does SMT differ from these types ?

10. Differentiate : GPUs and CPUs.

PART – B **(5×13=65 Marks)**

11. a) i) How are the generations of computers classified ? Give an overview of evolution of computer architectures from the first to the present generation. **(8)**

ii) Give a general expression to evaluate performance of a computer in terms of the number of instructions, operations and the clock frequency. Suggest a few architectural features using which this performance metric could be improved upon. **(5)**

(OR)

b) i) What is zero address instruction format ? Give an example. **(3)**

ii) Enumerate the most commonly used addressing modes of CPU instructions. **(6)**

iii) Registers R1 and R2 of a computer contain the decimal values 1200 and 4600. what is the effective address of the memory operand of the following instruction : Load 25(R1), R5. **(4)**

12. a) i) Show that the subtraction of an n-bit subtrahend from an n-bit minuend could be performed by addition operation with a suitable example. **(6)**

ii) State the purpose of Look Ahead Carry Adder. Derive the expressions for propagate and generate functions of a 4-bit Look Ahead Carry Adder and draw its schematic. **(7)**

(OR)

b) i) Consider a 32-bit floating point representation number system. What are the regions in which the numbers are not included in the range of numbers in such representation ? **(6)**

ii) Perform multiplication of integers 14 and –7 using Booth's multiplication algorithm. **(7)**

13. a) i) Explain the internal organization of a single-bus processor with a neat sketch showing the internal bus connecting the building blocks. **(8)**

ii) Distinguish between the visible and invisible registers available in processor organizations with specific examples. **(5)**

(OR)

b) i) Show that a five stage pipelined architecture would achieve a considerable saving on the execution time over that of a non-pipelined architecture with a neat sketch of timing diagram. Assume that all the stages viz. OF, ID, OR, EX and OW spend one unit of time for all the instructions. Determine the speed up achievable by the pipelined architecture in the absence of hazards of any types. **(8)**

ii) List the types of hazards and briefly explain the impact of such hazards on the performance of the pipelines. **(5)**

14. a) i) How does a DRAM differ from that of SRAM ? State the need for the refresh logic in DRAMs. **(5)**

ii) In a hierarchical memory system, where does the cache memory placed ? Explain the terms 'locality of reference' and 'cache line'. **(8)**

(OR)

b) i) Distinguish between the strobed I/O and interrupt driven data transfer modes. **(5)**

ii) What is the use of Translation Lookaside Buffers in Virtual Memory organization ? With a neat sketch explain the organization of associative-mapped TLB. **(8)**

15. a) i) Classify the computer architectures according to the Flynns taxonomy and write a brief note on level of parallelism achievable on these types of architectures. **(6)**

ii) Write detailed notes on Multiprocessor Network Topologies. **(7)**

(OR)

b) i) Explain the concept of cluster architecture with Google Server as an example. **(6)**

ii) Enumerate the types of network topologies and depict all such topologies pictorially for the interconnection of 8 nodes. **(7)**

PART – C **(1×15=15 Marks)**

16. a) i) Consider the following analogy of the concept of caching : A serviceman visits a house for a repair work. He uses the tools in the toolbox that he carried until he is in need of a tool which is not in the box. There is a chance that the required tool is available in the vehicle that he came from his office; if not he has to go to his office to bring the required tool to complete the work.

Suppose we argue that the toolbox, the vehicle and the office resemble that of L1, L2 cache and main memories of a computer, respectively. Is this a correct analogy ? Discuss its correct or incorrect features. **(8)**

ii) A disk unit has 24 recording surfaces. It has a total of 14,000 cylinders. There is an average of 400 sectors per track. Each sector contains 512 bytes of data. Determine the data transfer rate in bytessec at a rotational speed of 7200 rpm. Using a 32-bit word, suggest a suitable scheme for specifying the disk address, assuming that there are 512 bytes per sector. **(7)**

(OR)

b) Assume that a processor has 24-bit address bus and 8-bit data bus. Design a computer system that interfaces this processor with RAM of size 512 KB made of 64 KB chips and 64 KB of single chip ROM with address map starting at locations 400000 and 000000 respectively. Draw a neat sketch of the schematic diagram showing the interconnections and the address decoder. **(15)**

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Question Paper Code : 40450

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2021.

Fifth Semester

Electronics and Communication Engineering

EC 8552 – COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to B.E. Electronics and Telecommunication Engineering)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List the difference between wall clock time and response time.

2. Find the cycle time of a 450MHz clock frequency.

3. What is underflow in floating point arithmetic?

4. Write the expression for double precision number available in IEEE 754 format.

5. In a data path diagram, what is the size of ALUop control signal?

6. How PCSrc signal generated in a data path diagram?

7. In memory organization, what is temporal locality?

8. Considering memory hierarchy, define hit and miss.

9. Define fine-grain multithreading.

10. List the benefits of clustering in a computer architecture.

PART B — (5 × 13 = 65 marks)

11. (a) What is the role of each idea in the design of computer architecture? Explain. each of them with suitable examples. (4+9)

Or

(b) Explain about the central processing unit performance and its factors.(13)

12. (a) Determine the floating point multiplication of two numbers 2.5×10^8 and 8.0×10^{-3}. In this regard neatly sketch the corresponding flowchart too. (10+3)

Or

(b) How the division hardware is refined to speed up the division operation? Explain with diagrams. (4+9)

13. (a) What do you mean by hazards and what are the pipelining hazards occurs in a computer architecture? Describe each of them with suitable example. (3+10)

Or

(b) Build a suitable Data path for branch instruction. Explain all the blocks with suitable example. (6+7)

14. (a) What is cache memory? How to improve cache performance? Explain. (3+10)

Or

(b) What is virtual memory? Explain in detail about the virtual memory with suitable diagram. (3+10)

15. (a) What is hardware multi-threading? Explain different types of multi-threading occurs in parallel architectures. (3+10)

Or

(b) What is Graphics Processing Unit (GPU) and How GPUs can be distinguished from CPUs? Neatly sketch the GPU memory structure which is shared by vectorized loops. Explain briefly. (6+7)

PART C — (1 × 15 = 15 marks)

16. (a) Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2. Given a program with a dynamic instruction count of 1000 instructions divided into classes as follows: (15)

10% class A, 20% class B, 50% class C, and 20% class D.

(i) Find the clock cycles required in both cases.

(ii) Which implementation is faster and how much?

Or

(b) Discuss on the concept and applications of clusters and warehouse scale computers.

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Question Paper Code : 70518

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2023.

Fifth Semester

Electronics and Communication Engineering

EC 8552 – COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to Electronics and Telecommunication Engineering)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Differentiate execution time and throughput.

2. List the uses of instruction register and program counter.

3. State the two ways detect overflow in an n-bit adder.

4. Give an example for the worst case of Booth's algorithm.

5. What are the major characteristics of a pipeline?

6. Differentiate imprecise and precise exception.

7. Can IO devices be connected directly to the system bus? Give reasons.

8. Define data stripping.

9. Name two methods of achieving parallelism.

10. Compare warehouse scale computers with data centers.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Differentiate shared memory multiprocessors and distributed memory multi computers. (8)

(ii) Explain how performances gain is calculated using Amdahl's law. (5)

Or

(b) (i) Explain the Flynn's classification of computer architecture. (8)

(ii) How is register direct addressing mode different from register indirect addressing mode? (5)

12. (a) (i) List the steps for performing restoring division and non-restoring division. (8)

(ii) State the advantages of non-restoring over restoring division. (5)

Or

(b) (i) Explain floating point representation with an example. (8)

(ii) Name the 2 IEEE standards for the floating point numbers. (5)

13. (a) With diagrams, explain the pipelined execution of successive instructions in a base scalar processor and in two under pipelined cases. (13)

Or

(b) Explain how data hazards are overcome by dynamic scheduling using Tomasulo's algorithm. (13)

14. (a) (i) Explain various techniques used for the reduction of miss penalty and miss rate. (7)

(ii) Discuss the protection mechanism used for virtual memory. (6)

Or

(b) (i) Explain the three types of internal communication methodologies. (7)

(ii) Write short notes on RAID structure. (6)

15. (a) (i) List the challenges of parallel processing architecture. (7)

(ii) Illustrate the concept of Hardware multithreading. (6)

Or

(b) Explain the classification of multiprocessor network topologies based on their topological properties. (13)

PART C — (1 × 15 = 15 marks)

16. (a) (i) With state diagrams, explain the transition diagram for a pipeline unit. (8)

(ii) Explain the pipelined execution for the given instructions : (7)

- $X = Y + Z$
- $A = B \times C$

Or

(b) (i) With a flowchart, explain the algorithm for performing floating point multiplication. (7)

(ii) Differentiate cache memory and virtual memory. (8)