SNS COLLEGE OF TECHNOLOGY

Coimbatore-35

An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A++' Grade

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

23ECB222- Digital Principles and Computer Organization

II AIML / III SEMESTER

UNIT 2 – Combinational Circuits

Full Adder

A combinational logic circuit that can add two binary digits (bits) and a carry bit, and produces a sum bit and a carry bit as output is known as a **full-adder**.

- The first two inputs are A and B and the third input is an input carry as C-IN.
- The output carry is designated as C-OUT and the normal output is designated as S which is SUM.

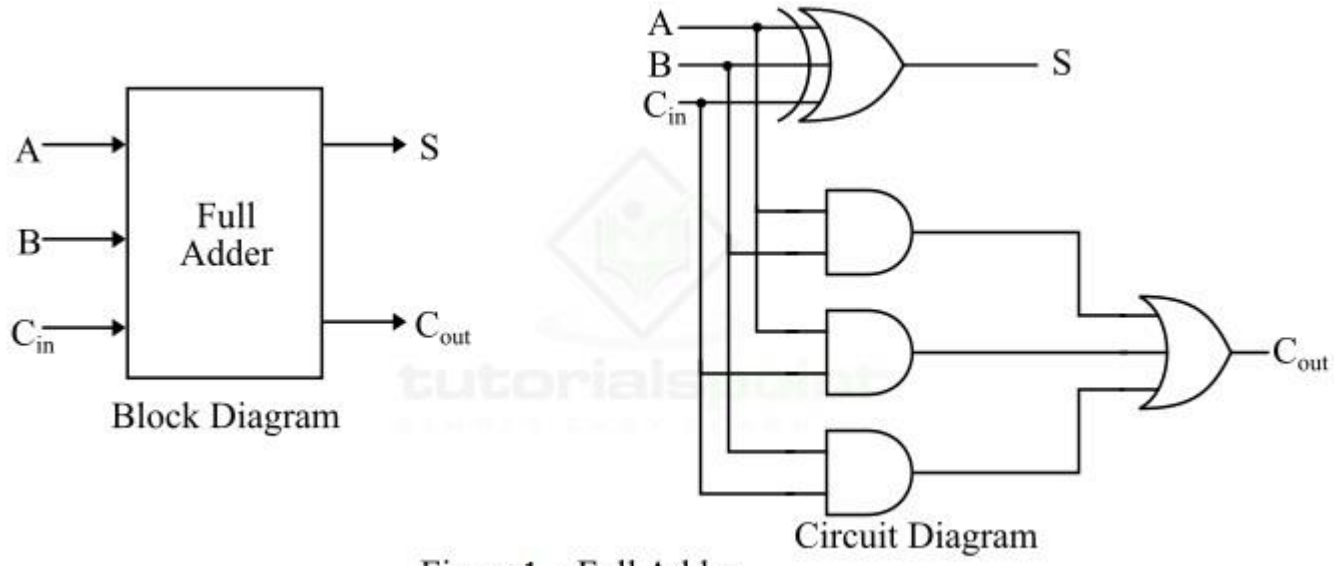

Figure 1 - Full Adder

Truth table

Inputs			Outputs	
A	B	C – IN	Sum	C - Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K- Map for full adder

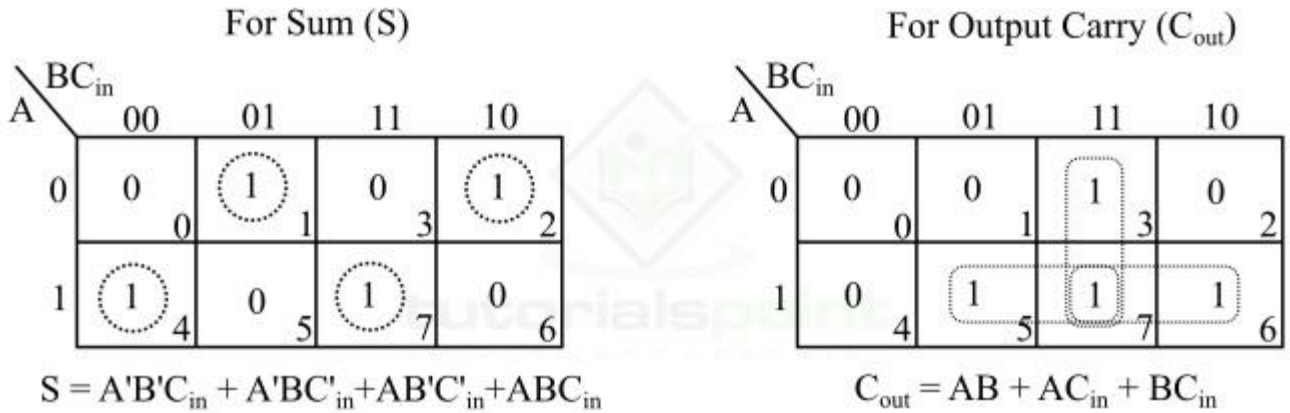

Figure 2 - K Map for Full Adder

Sum,S=A⊕B⊕Cin=A′B′Cin+A′BC′in+AB′C′in+ABCin

Carry,C=AB+ACin+BCin

Application of Half Adder in Digital Logic

- ALUs (arithmetic logic units) of CPUs of computers.
- It is used in calculators.
- It also helps in carrying out multiplication of binary numbers.
- It is used to realize critic digital circuits like multiplexers.
- To generate memory addresses.
- Full adders are also used in GPU (Graphical Processing Unit).

THANK YOU