SNS COLLEGE OF TECHNOLOGY

Coimbatore-35.

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COURSE NAME : 23ITT202 – COMPUTER ORGANIZATION AND ARCHITECTURE

II YEAR/ III SEMESTER

UNIT – I OVERVIEW AND INSTRUCTION

Topic: Memory Locations and Addresses

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Memory locations and addresses

The memory consists of many million of storage **cells**, each of which can store a bit o information having the value 0 or 1.

The memory is organized so a group of n bits can be stored or retrieved in a single basic operation.

Each group of **n bits** is referred to as a word of information, and n is called the **word length**.

A unit of 8 bits is called a **byte**.

Accessing the memory to store or retrieve a single item of information, either a word or a byte, requires distinct names or addresses for each item location.

2^k addresses constitute the address space from 0 to $2^k – 1$, for some suitable value of k.

For example, a 32-bit address creates an address space of 2^{32} or 4G (4 giga) locations.

2^{32} = 4,294,967,296 bytes (4GB RAM)

2^{10} = 1 KB (kilo)	= 1024 bytes
1 MB (mega)	= 1024 KB
1 GB (giga)	= 1024 MB
1 TB (tera)	= 1024 GB
1 PB (peta)	= 1024 TB

Byte Addressability

A byte is always 8 bits, but the word length typically ranges from 16 to 64 bits.

It is impractical to assign distinct addresses to individual bit locations in the memory. The most practical assignment is to have successive addresses refer to successive byte locations in the memory.

If the word length of the machine is 32 bits, successive words are located at addresses 0,4,8,…, with each word consisting of four bytes.

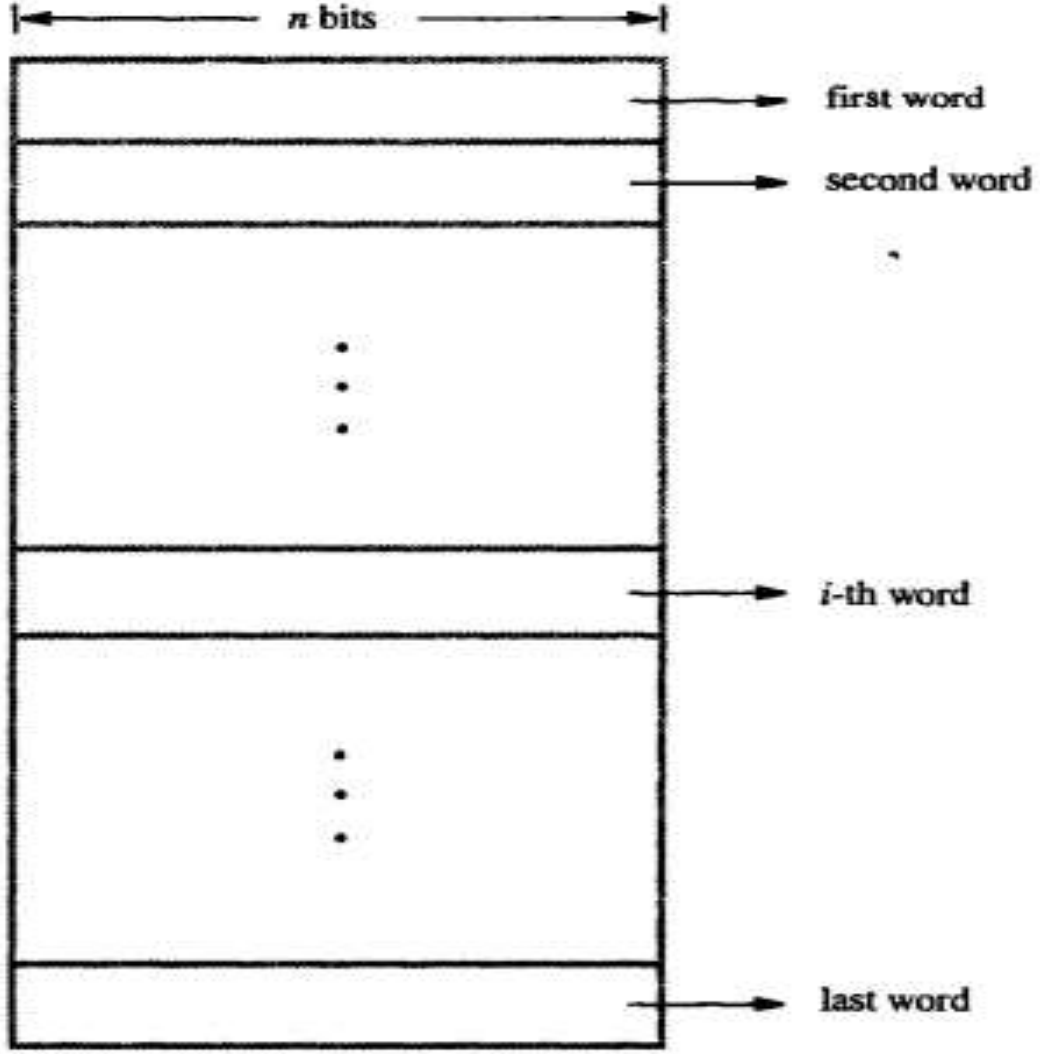


Figure 2.5 Memory words.

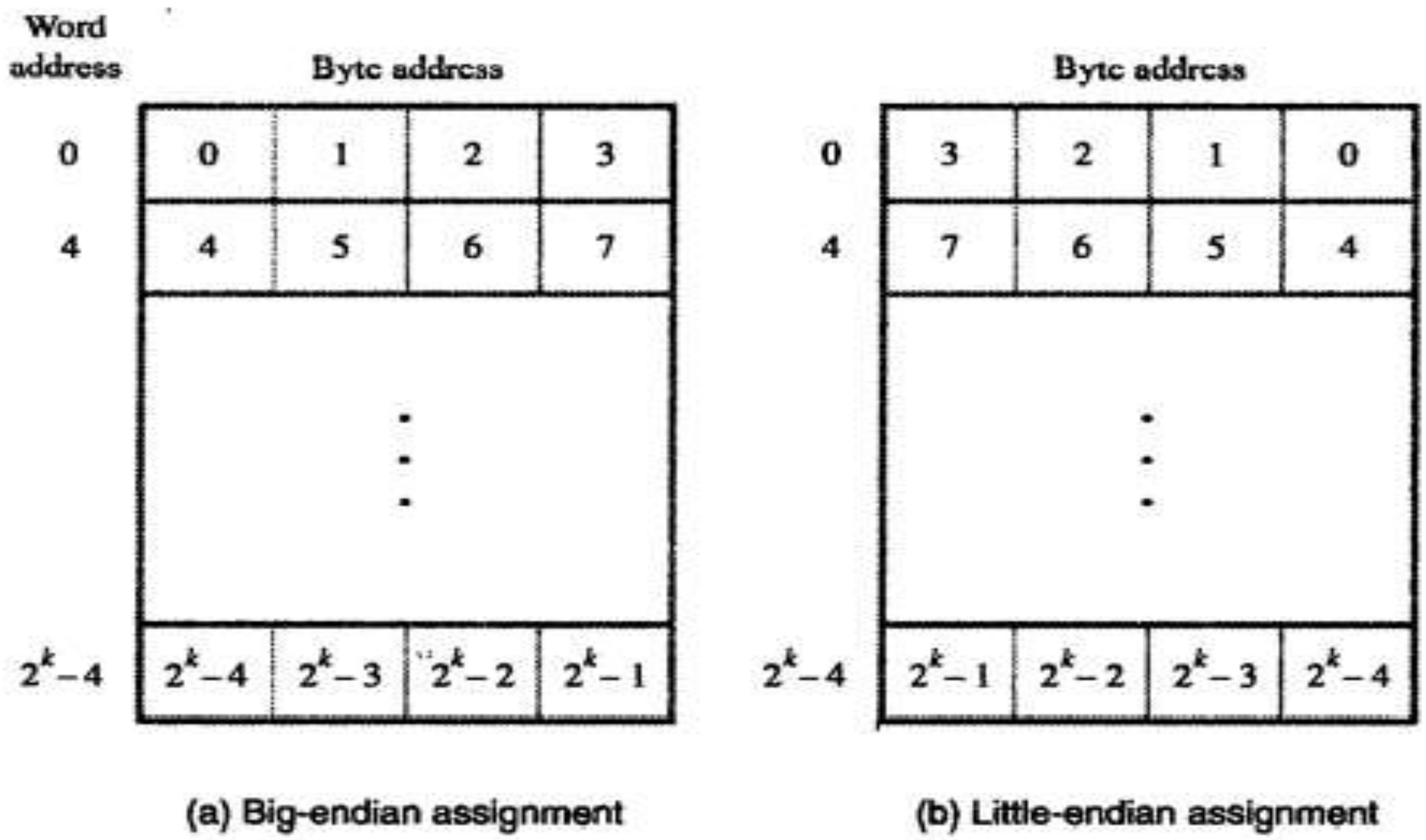
Big-endian & Little-endian Assignments

There are two ways that the byte addresses can be assigned across words.

The name big-endian is used when lower byte addresses are used for t he more significant bytes (the leftmost bytes) of the word.

The name little-endian is used for the opposite ordering, where the lower byte addresses are used for the less significant bytes (the rightmost bytes) of the word.

Word Alignment



Word address	Byte address			
0	0	1	2	3
4	4	5	6	7
	⋮			
2^k-4	2^k-4	2^k-3	2^k-2	2^k-1

(a) Big-endian assignment

	Byte address			
0	3	2	1	0
4	7	6	5	4
	⋮			
2^k-4	2^k-1	2^k-2	2^k-3	2^k-4

(b) Little-endian assignment

Figure 2.7 Byte and word addressing.

Memory Operations

Two basic operations

→ Load (Read/Fetch)

→ Store (Write)

To execute an instruction, the processor control circuits must cause the word containing the instruction to be transferred from the memory to the processor.

Operands & results must also be moved between the memory and the processor.

Thus, two basic operations involving the memory Load & Store are needed.

Load operation

The load operation transfers a copy of the contents of a specific memory location to the processor.

The memory contents remain unchanged.

Load operation involves-

→ The processor sends the address of the desired location to the memory and requests its contents to read.

→ The memory reads the data stored at that address and sends them to the processor.

Store operation

The store operation transfers an item of information from the processor to a specific memory location, by destroying the former contents of that location.

Store operation involves-

→ The processor sends the address of the desired location to the desired location to the memory, together with the data to be written into that location.

THANK YOU!

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