SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A+' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB302–VLSI DESIGN

III YEAR/ V SEMESTER

UNIT 3 –SEQUENTIAL LOGIC CIRCUITS
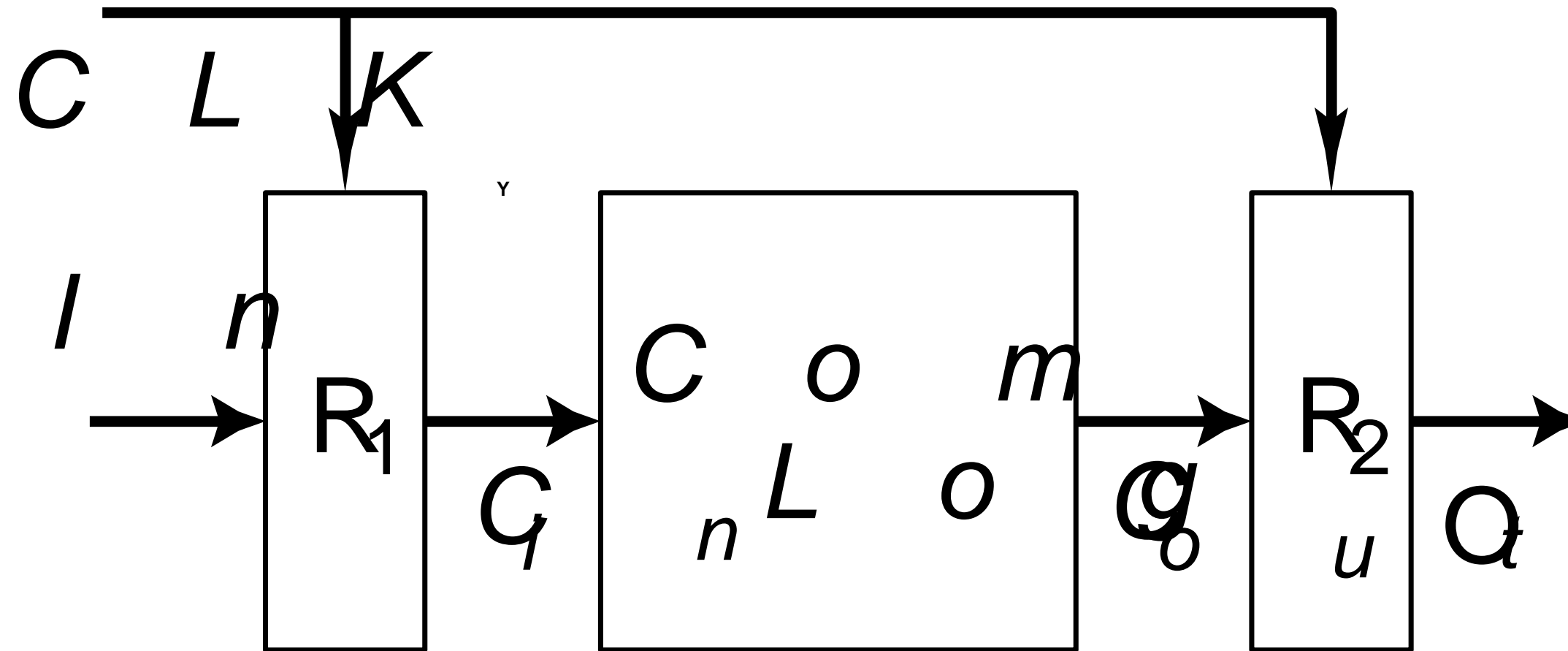
TOPIC 3 –TIMING ISSUES

OUTLINE

- **SYNCHRONOUS TIMING**
- **LATCH PARAMETERS**
- **REGISTER PARAMETERS**
- **CLOCK UNCERTAINTIES**
- **CLOCK NONIDEALITIES**
- **CLOCK SKEW AND JITTER**
- **POSITIVE AND NEGATIVE SKEW**
- **TIMING CONSTRAINTS**
- **ACTIVITY**
- **IMPACT OF JITTER**
- **SHORTEST PATH**
- **HOW TO COUNTER CLOCK SKEW?**
- **LATCH TIMING**
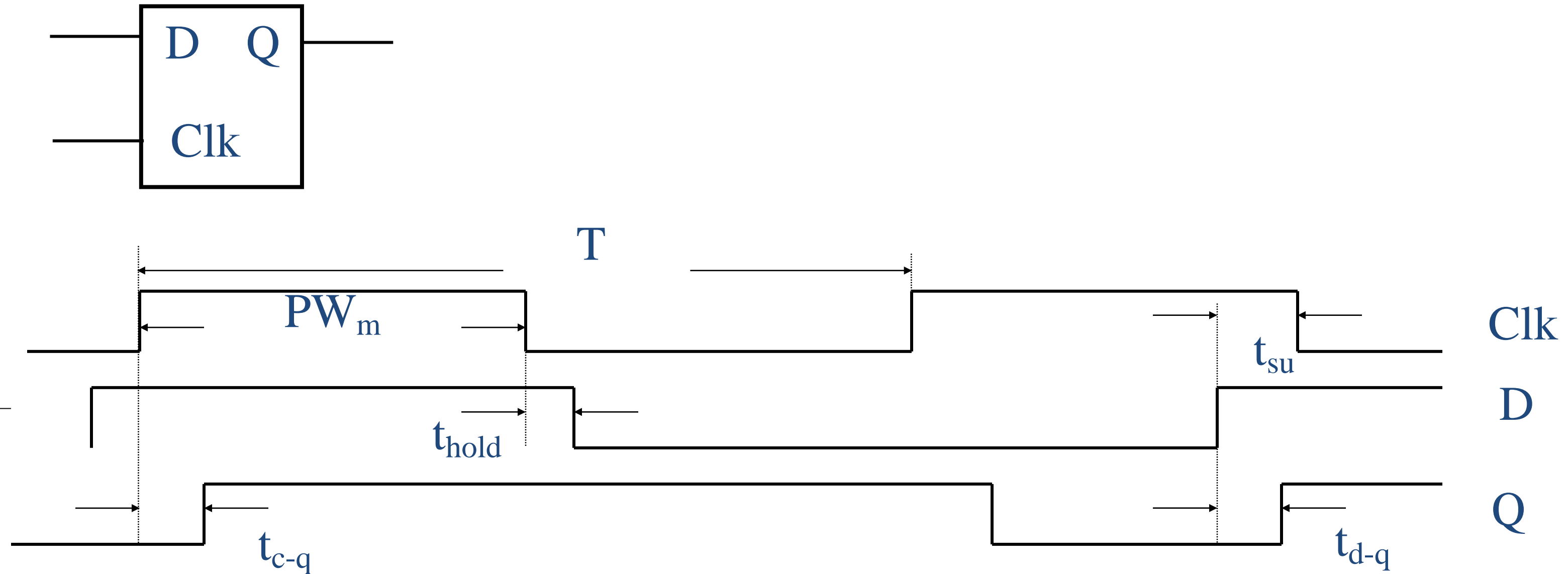- **ASSESSMENT**
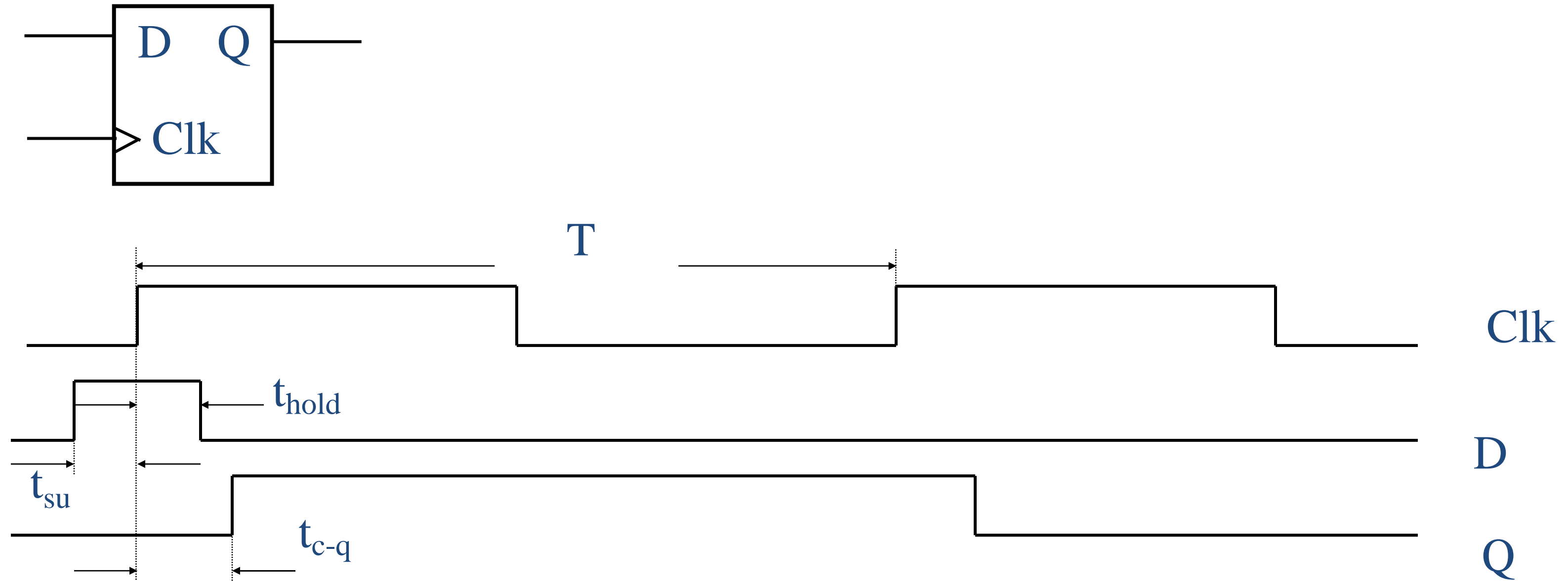- **SUMMARY & THANKYOU**

SYNCHRONOUS TIMING

Delays can be different for rising and falling data transitions

REGISTER PARAMETERS

Delays can be different for rising and falling data transitions

CLOCK UNCERTAINTIES

CLOCK NONIDEALITIES

- **Clock skew**
  - Spatial variation in temporally equivalent clock edges; deterministic + random, t_{SK}
- **Clock jitter**
  - Temporal variations in consecutive edges of the clock signal; modulation + random noise
  - Cycle-to-cycle (short-term) t_{JS}
  - Long term t_{JL}
- **Variation of the pulse width**
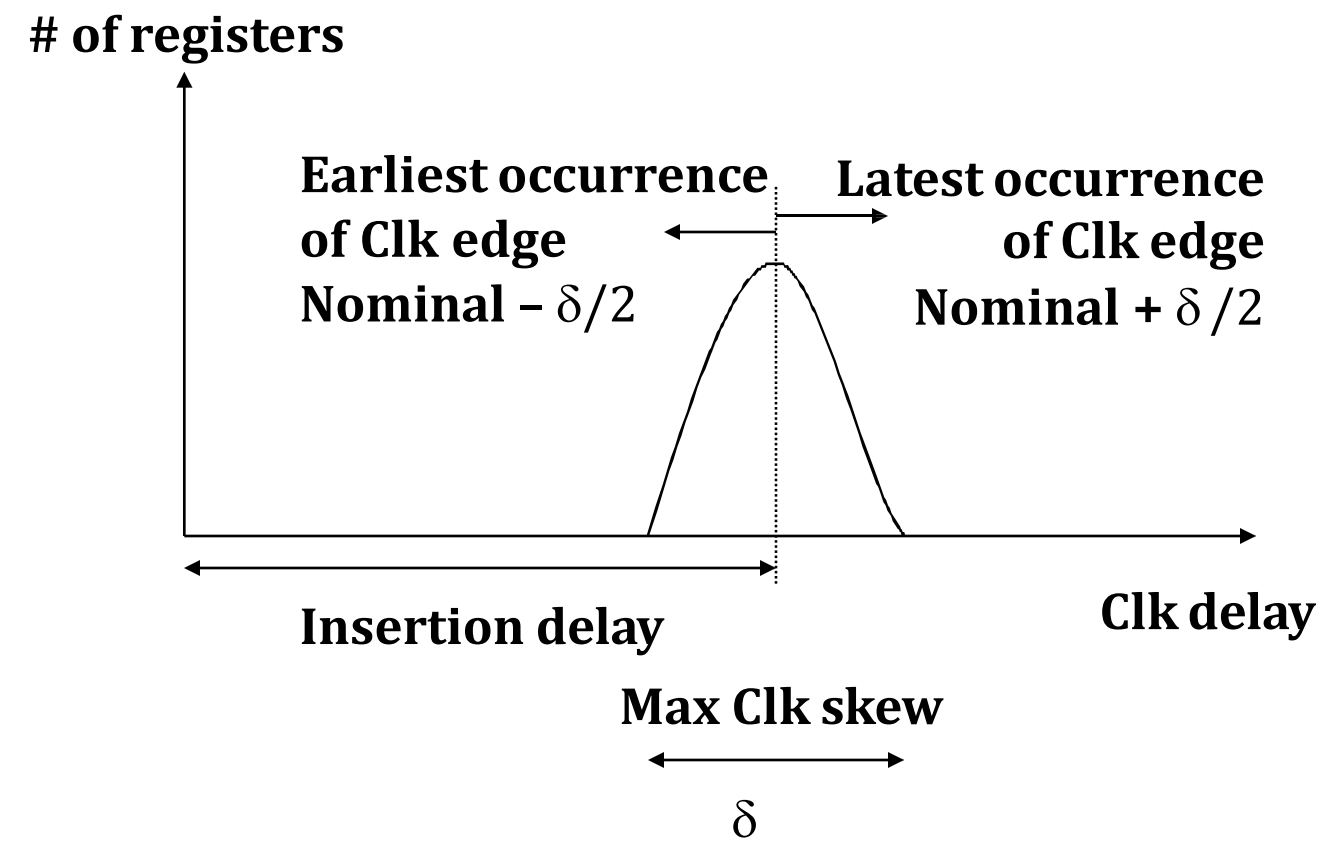 - Important for level sensitive clocking

CLOCK SKEW AND JITTER
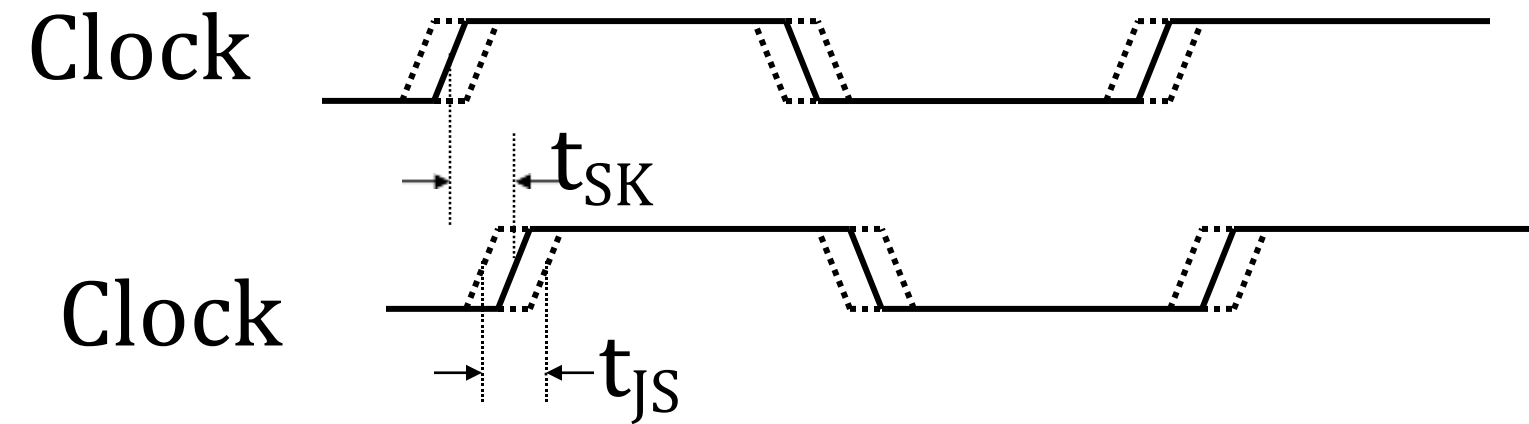
- Both skew and jitter affect the effective cycle time
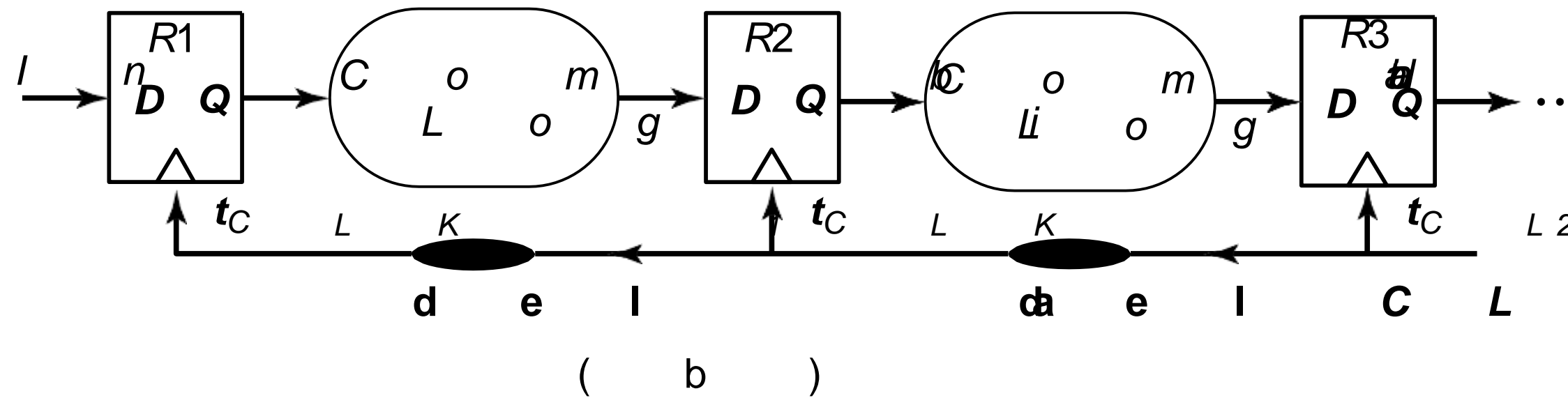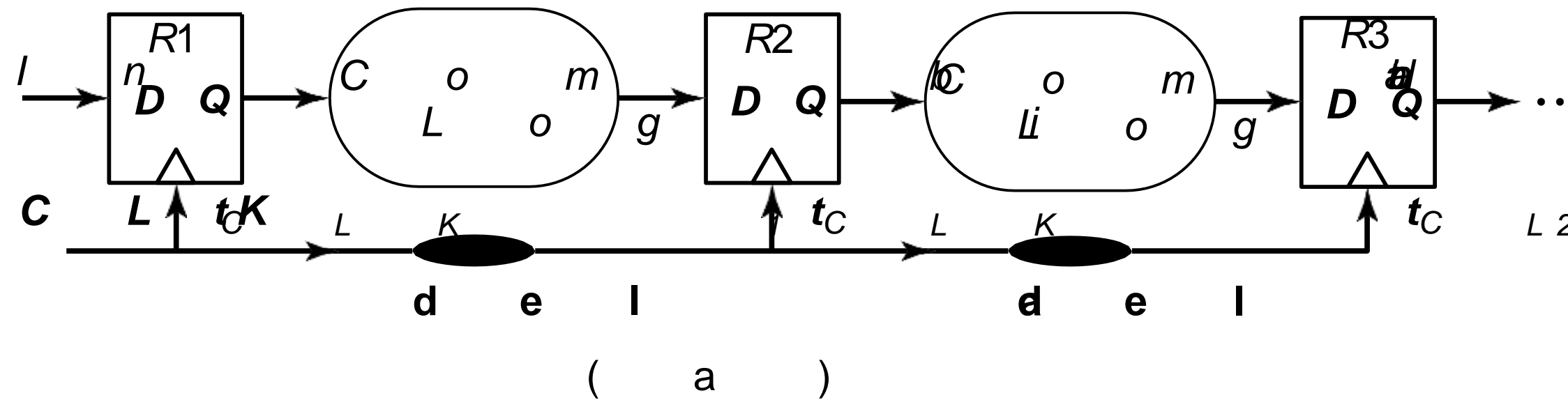- Only skew affects the race margin

CLOCK SKEW

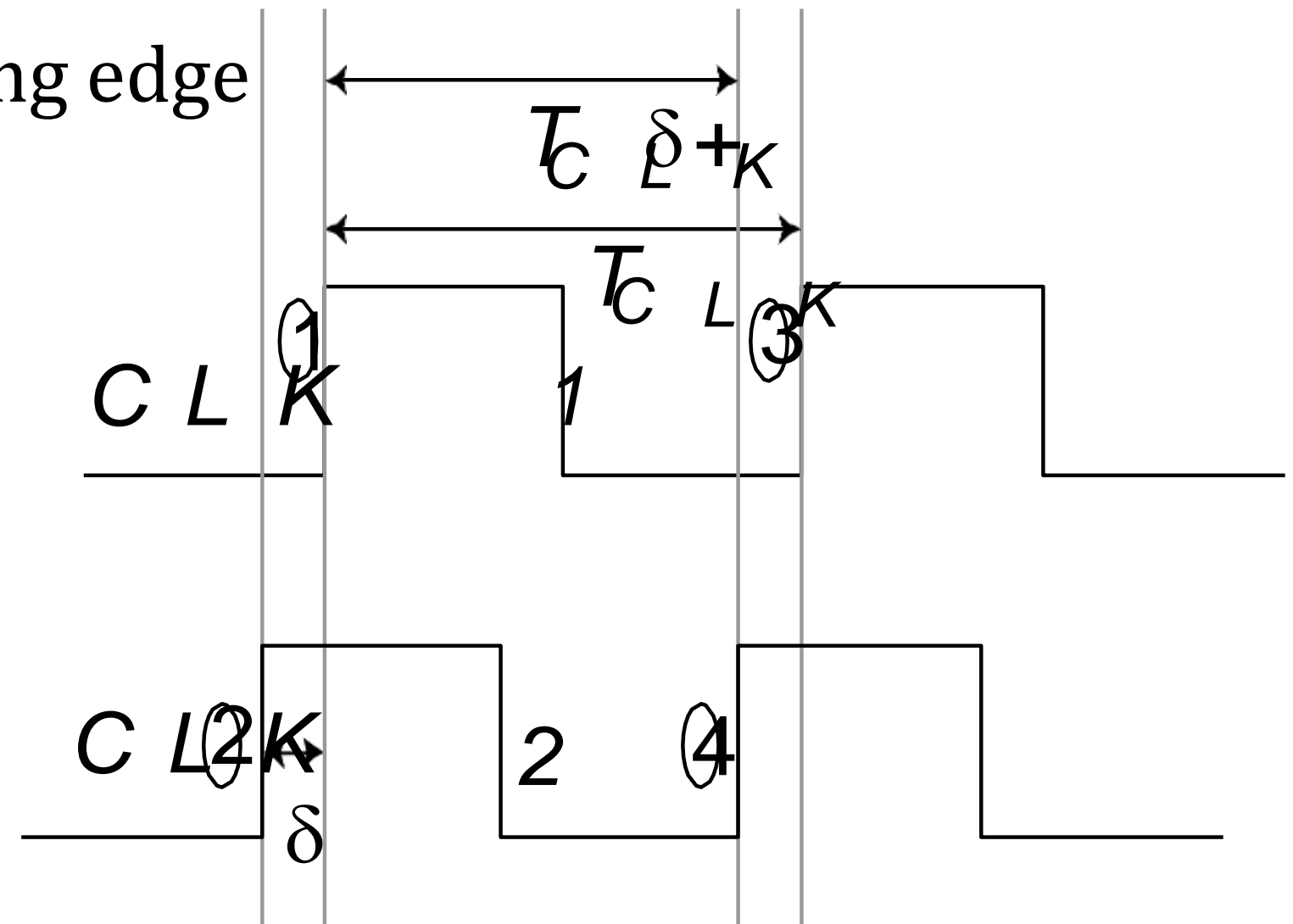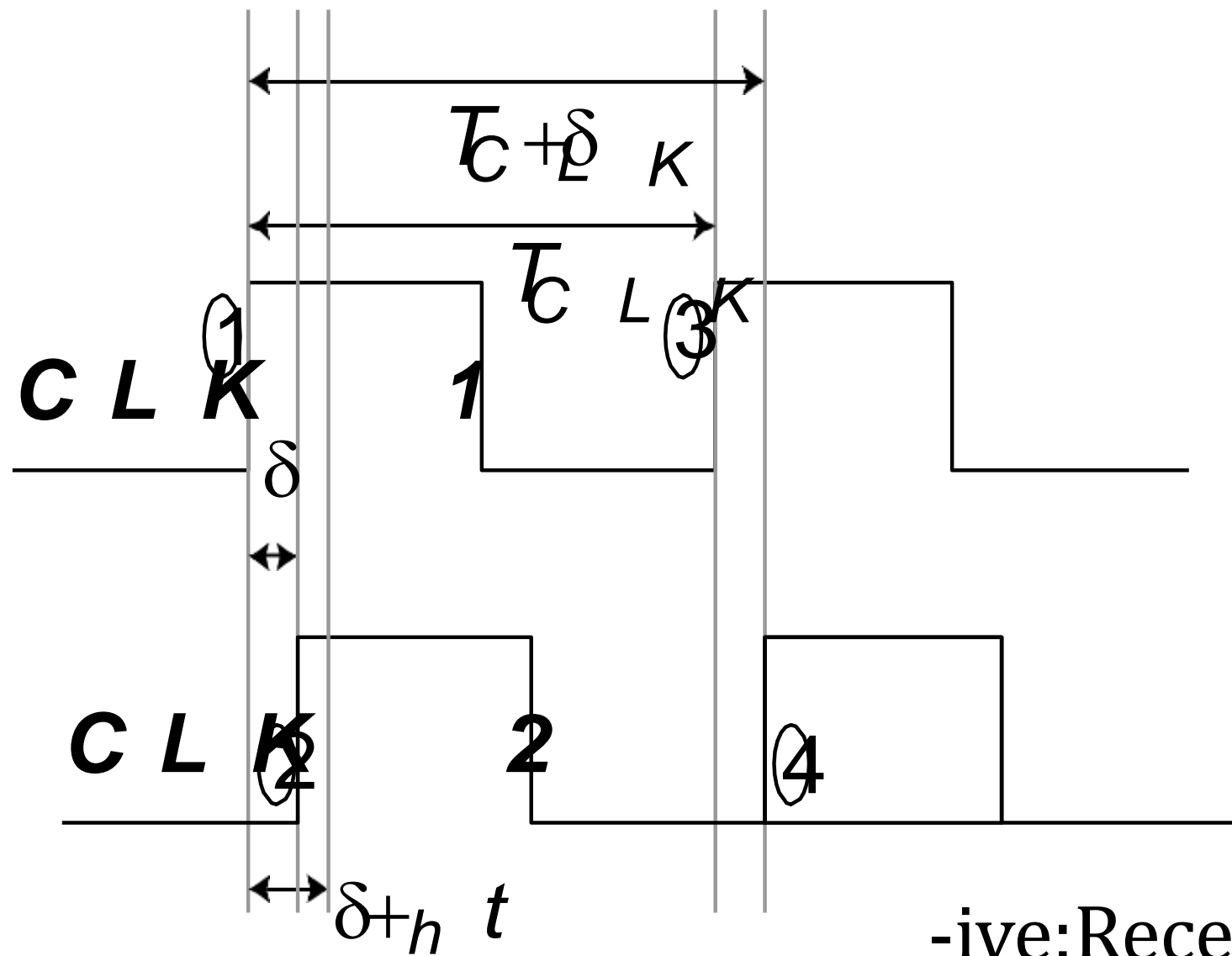# POSITIVE AND NEGATIVE SKEW

(a)

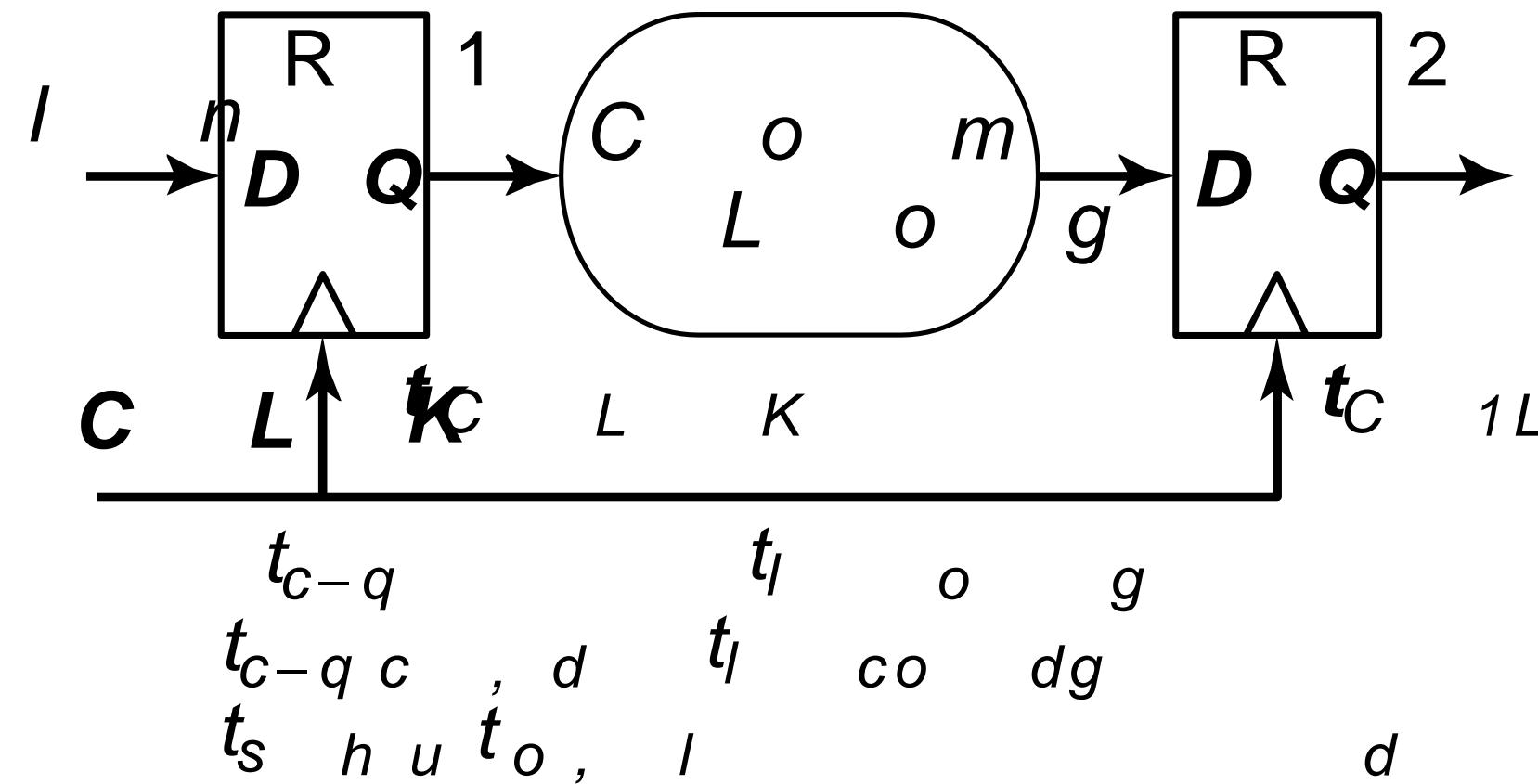

(b)

POSITIVE SKEW & NEGATIVE SKEW

Launching edge arrives before the receiving edge

-ive:Receiving edge arrives before the launching edge

TIMING CONSTRAINTS

Minimum cycle time:

$$T - \delta = t_{c\text{-}q} + t_{su} + t_{logic}$$

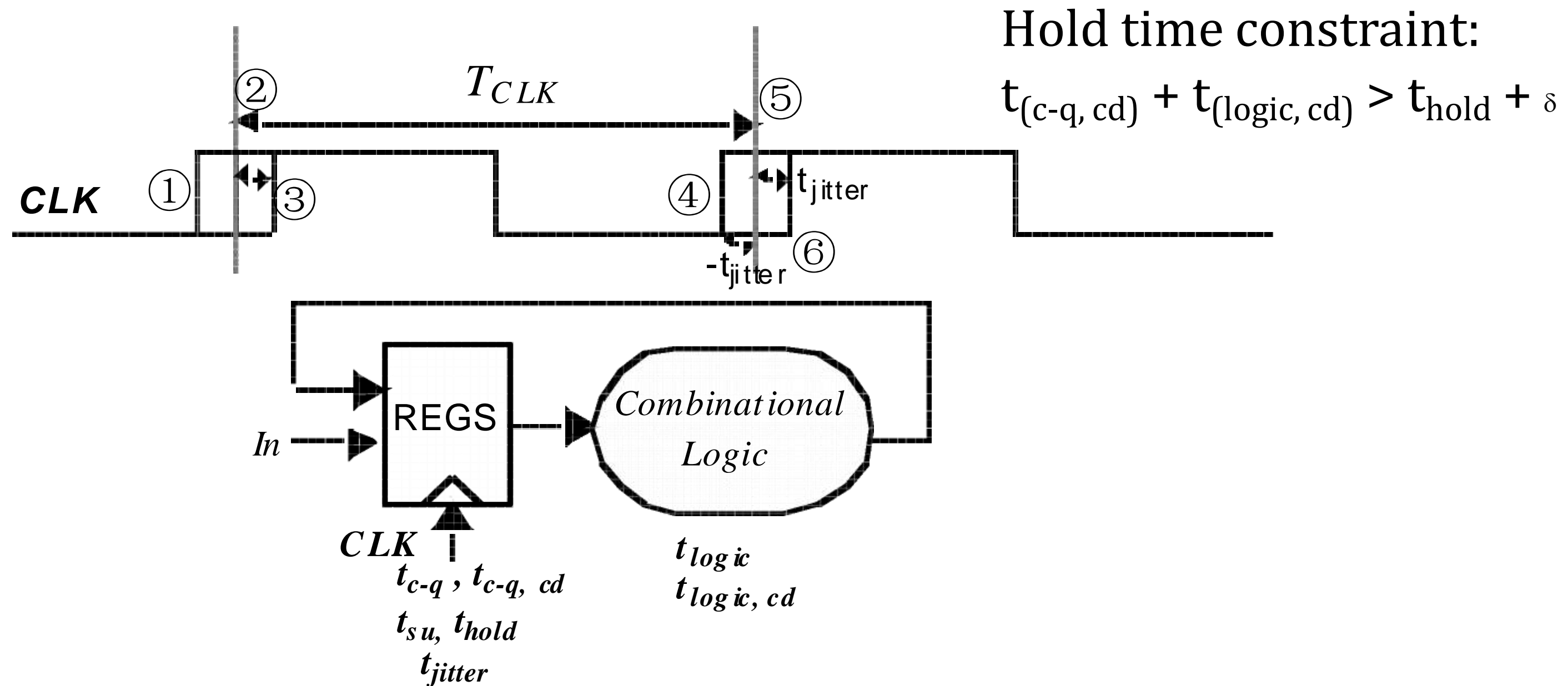Worst case is when receiving edge arrives early (positive δ)

STUDY THE PYRAMID CAREFULLY.

E

1110   D

446   679   681

198   263   431   265

WHAT ARE THE VALUES OF E AND D?

IMPACT OF JITTER

Hold time constraint:

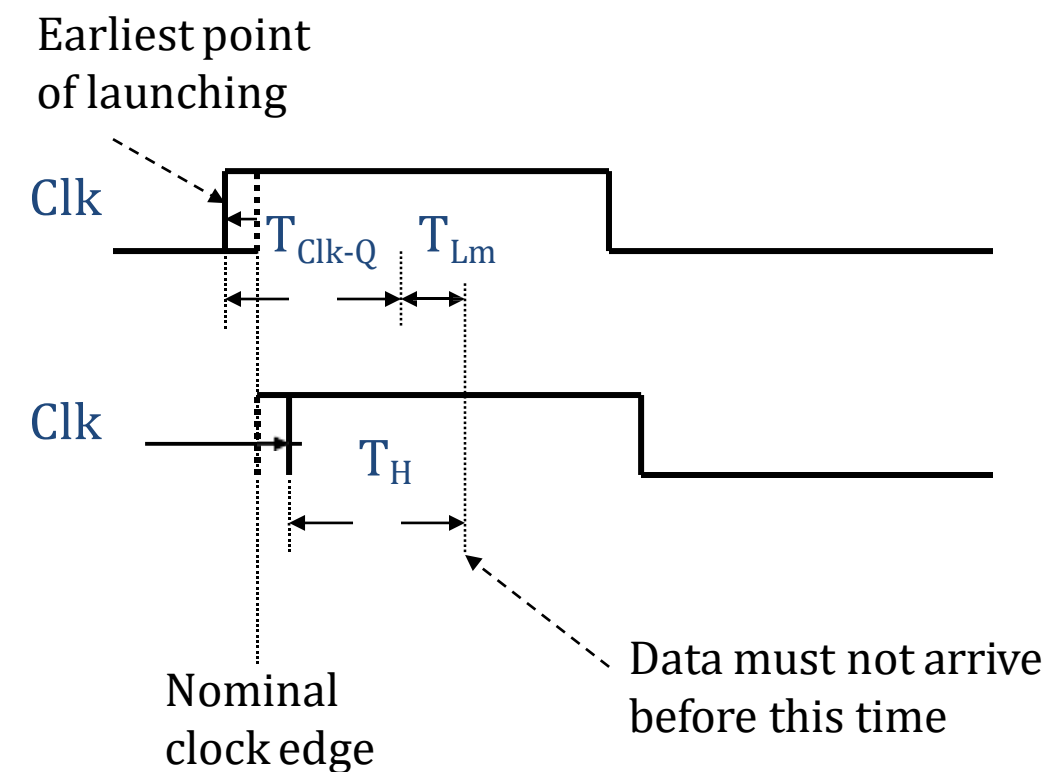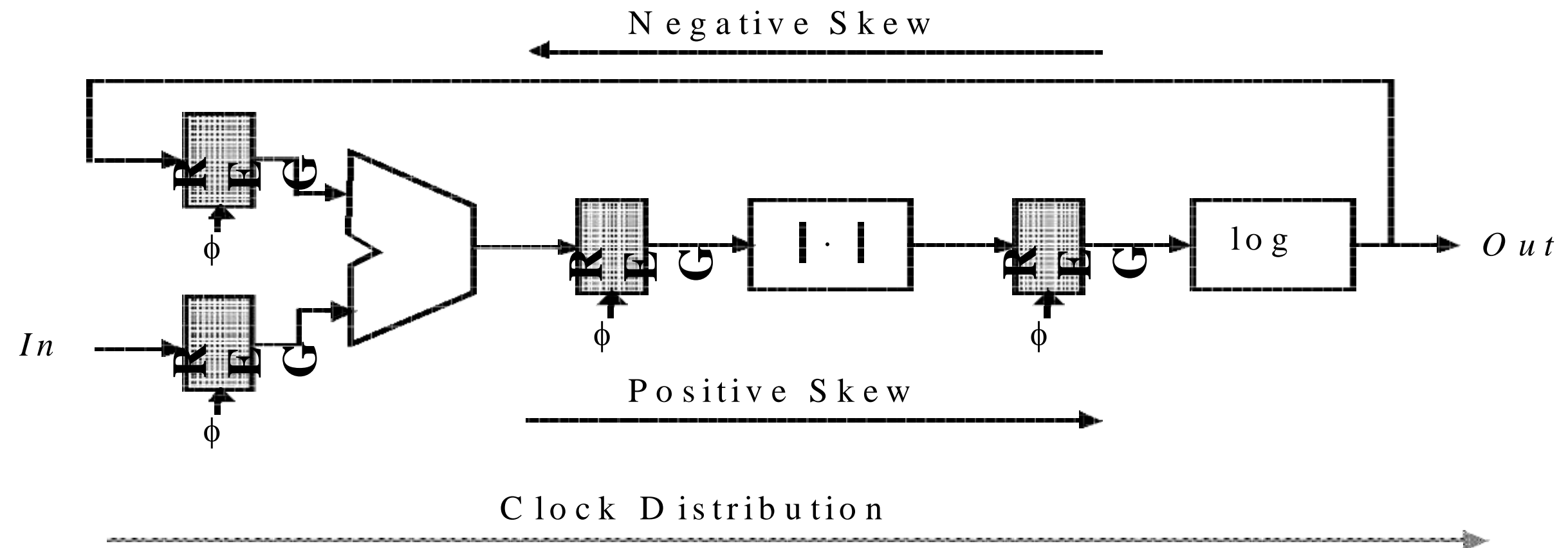$$t_{(c\text{-}q,\, cd)} + t_{(logic,\, cd)} > t_{hold} + \delta$$

Worst case is when receiving edge arrives late
Race between data and clock

HOW TO COUNTER CLOCK SKEW?

Data and Clock Routing

LATCH TIMING

•When data arrives
•to closed latch

•Data has to be 're-launched'

t_{D-Q}

$$\boxed{\begin{array}{cc} D & Q \\ & \\ Clk & \end{array}}$$

t_{Clk-Q}
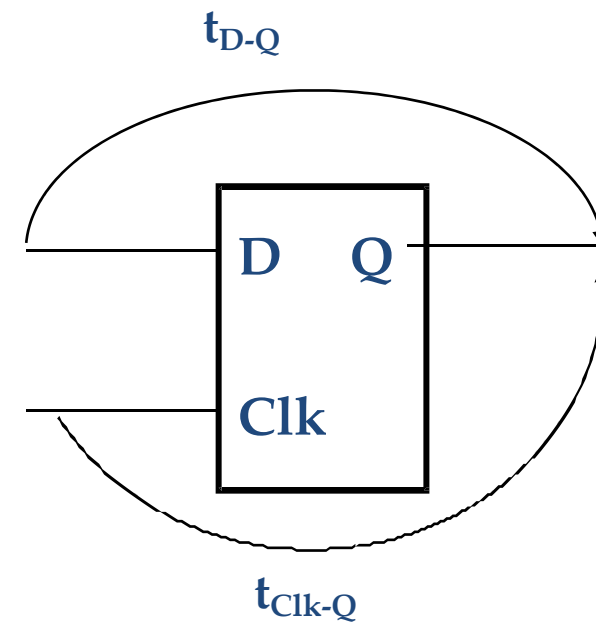
•Latch is a 'soft' barrier

•When data arrives
to transparent latch

1. Compare latch & Register parameters

2. Define Clock Skew & Jitter

3. Differentiate positive skew & negative skew

4. How to counter clock skew**?**

SUMMARY & THANK YOU