SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A+' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB302–VLSI DESIGN

III YEAR/ V SEMESTER

UNIT 4 –VLSI TESTING

TOPIC 8,9 –CHIP LEVEL TEST TECHNIQUES &

SYSTEM LEVEL TEST TECHNIQUES.

OUTLINE

- SYSTEM-LEVEL TEST TECHNIQUES INTRODUCTION
- BASIC CONCEPT OF TESTING
- BOUNDARY SCAN-OPERATION MODES
- SYSTEM-LEVEL OPERATION
- SYSTEM-LEVEL TESTING
- TEST GENERATION
- FAULT MODELS
- ELECTRONIC SYSTEM MANUFACTURING
- ACTIVITY
- CHIP LEVEL TESTING
- ASSESSMENT
- SUMMARY & THANK YOU

SYSTEM-LEVEL TEST TECHNIQUES INTRODUCTION

- In the **1970s, the in-circuit testing (ICT) method appeared.**
- Mechanical testing becomes difficult with board trace widths ard separations below 0.1 mm or 100 Jam. below 0.1 mm or 100 Jam.
- **In 1985 a group of European manufacturer formed** the Joint European Test Action Group (JETAG) to study board testing.
- **In 1986 JETAG becomes Joint Test Action Group (JTAG)** with the addition of North American Companies.. The main virtue of the 1149.1 standard can be used by board designers, IC designers, and systems designers.
- without the need for members of each design community to fully understand the testing problems of the other communities.

BOUNDARY SCAN: MAJOR MODES OF OPERATION

- Boundary scan is actually a collection of design rules, applied at the IC level for testing hoards using a four-wire interface (five wires with an optional master reset signal).

•Boundary scan provides the following major modes of operation:

- These resources enable asynchronous communication with the outside world to serially read in test data and instructions or serially read out test results.

- The activities are invisible to the normal IC behaviour.

- The pin-permission modes of the standard take control of the IC input/output pins, thus disconnecting the system logic from the outside world.

- These modes allow testing of the system interconnect separately from component testing.. And also allow testing of components separately from system interconnect testing.

- The testing activities totally disrupt the normal IC behaviour. The testing activities totally disrupt the normal IC behaviour.

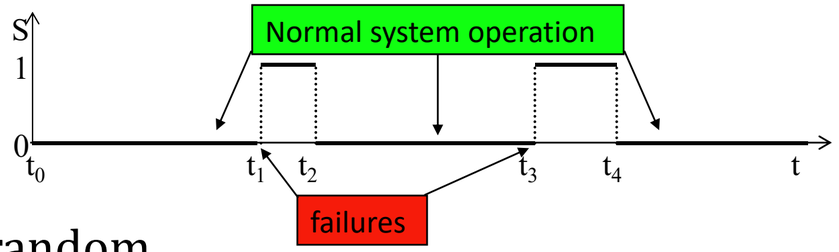
BOUNDARY SCAN DESCRIPTION LANGUAGE

•The Boundary scan Description Language (BSDL) was added to the JTAG Boundary scan standard to provide a standard means of communicating information about the boundary scan hardware on a chip to users of the chip and to CAD tools through the VHDL hardware description language.

• BSDL can b used by automatic test-pattern generator to generate chip test pattern, and by high-level and logic synthesis tools to synthesize test logic.

SYSTEM-LEVEL OPERATION

- Faults occur
  during system operation
- Exponential failure law
  - Interval of normal system operation is random number exponentially distributed
- Reliability
  - Probability that system will operate normally until time *t*
  - Failure rate, λ, is sum of individual component failure rates, λ_i



SYSTEM-LEVEL OPERATION

- Mean Time Between Failures (MTBF)
- Repair time (R) also assumed to obey exponential distribution
  - μ is repair rate
- Mean Time To Repair (MTTR)
- Fraction of time that system is operating normally called system availability
  - High reliability systems have system availabilities greater than 0.9999
    - Referred to as “four 9s”

$$MTBF = \int_0^\infty e^{-\lambda t} dt = \frac{1}{\lambda}$$

$$P(R > t) = e^{-\mu t}$$

$$MTTR = \frac{1}{\mu}$$

$$system\ availability = \frac{MTBF}{MTBF\ +\ MTTR}$$

SYSTEM-LEVEL TESTING

- Testing required to ensure system availability
- Types of system-level testing
  - On-line testing – concurrent with system operation
  - Off-line testing – while system (or portion of) is taken out of service
    - Performed periodically during low-demand periods
    - Used for diagnosis (identification and location) of faulty replaceable components to improve repair time

HOW TO DO TESTING

From designer's point of view:

- **Circuit modeling**
- **Fault modeling**

} **Modeling**

- **Logic simulation**
- **Fault simulation**
- **Test generation**

} **ATPG**

- **Design for test**
- **Built-in self test**

} **Testable design**

- **Synthesis for testability**

TEST GENERATION

- A test is a sequence of test patterns, called test vectors, applied to the CUT whose outputs are monitored and analyzed for the correct response
  - Exhaustive testing – applying all possible test patterns to CUT
  - Functional testing – testing every truth table entry for a combinational logic CUT
    - Neither of these are practical for large CUTs
- Fault coverage is a quantitative measure of quality of a set of test vectors

TEST GENERATION

- Fault coverage for a given set of test vectors
- 100% fault coverage may be impossible due to undetectable faults

$$fault\ coverage = \frac{number\ of\ detected\ faults}{total\ number\ of\ faults}$$

$$fault\ detection\ efficiency = \frac{number\ of\ detected\ faults}{total\ number\ of\ faults - number\ of\ undetectable\ faults}$$

- $Reject\ rate = 1 - yield^{(1\ -\ fault\ coverage)}$
  - A PCB with 40 chips, each with 90% fault coverage and 90% yield, has a reject rate of 41.9%
    - Or 419,000 defective parts per million (PPM)

TEST GENERATION

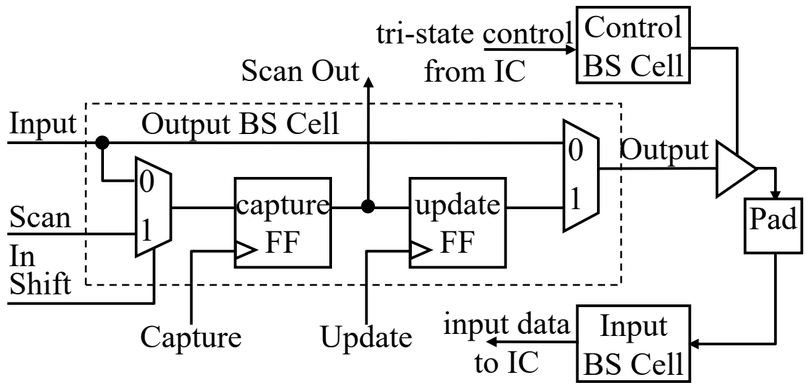
- *Goal*: find efficient set of test vectors with maximum fault coverage
- Fault simulation used to determine fault coverage
  - Requires fault models to emulate behavior of defects
- A good fault model:
  - Is computationally efficient for simulation
  - Accurately reflects behavior of defects
- No single fault model works for all possible defects

FAULT MODELS

- A given fault model has k types of faults
  - k = 2 for most fault models
- A given circuit has n possible fault sites
- Multiple fault model –circuit can have multiple faults (including single faults
  - Number of multiple fault = $(k+1)^n-1$
    - Each fault site can have 1-of-k fault types or be fault-free
    - The “-1” represents the fault-free circuit
  - Impractical for anything but very small circuits
- Single fault model – circuit has only 1 fault
  - Number of single faults = $k \times n$
  - Good single fault coverage generally implies good multiple fault coverage

BOUNDARY SCAN

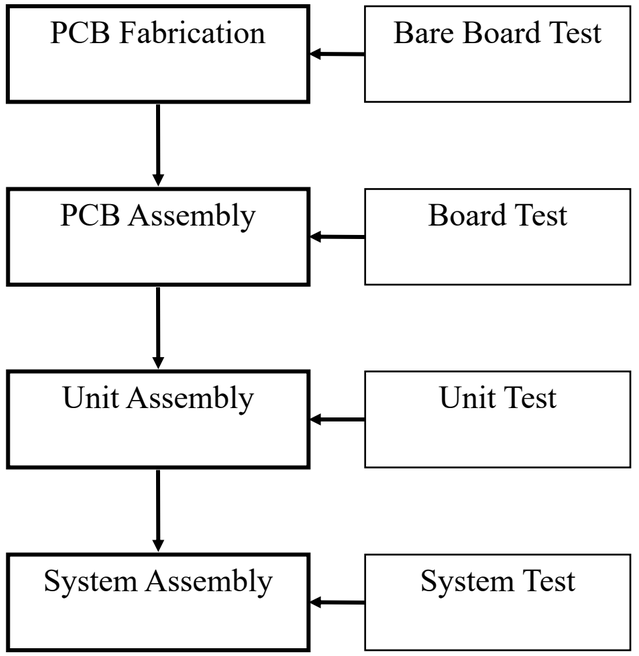
- Boundary Scan – scan design applied to I/O buffers of chip
  - Used for testing interconnect on PCB
    - Provides access to internal DFT capabilities
  - IEEE standard 4-wire Test Access Port (TAP)



TAP pin	I/O	Function
TCK	input	Test clock
TMS	input	Test Mode Select
TDI	input	Test Data In
TDO	output	Test Data Out

ELECTRONIC SYSTEM MANUFACTURING

- A system consists of
  - PCBs that consist of
    - VLSI devices
- PCB fabrication similar to VLSI fabrication
  - Susceptible to defects
- Assembly steps also susceptible to defects
  - Testing performed at all stages of manufacturing



CLASS ROOM ACTIVITY

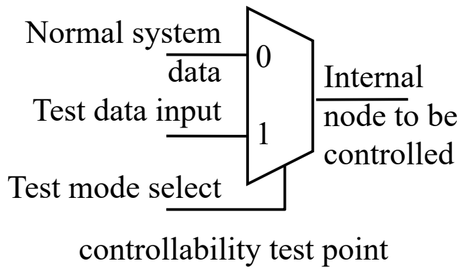
DEBATE

CHIP LEVEL TESTING

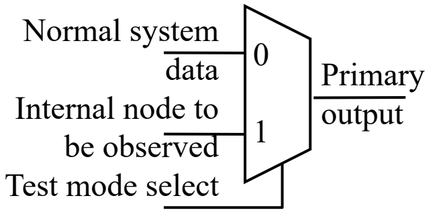
Design for Testability (DFT)

Generally incorporated in design

Goal: improve controllability and/or observability of internal nodes of a chip or PCB



controllability test point

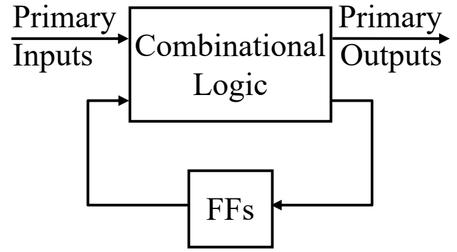


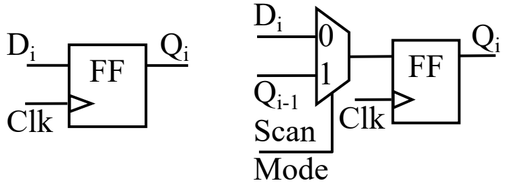
observability test point

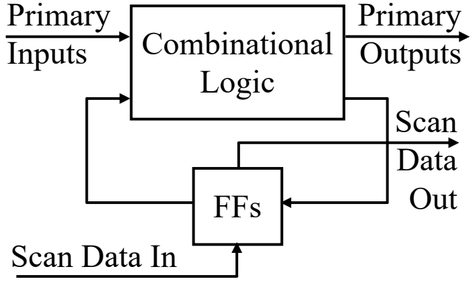
- Ad-hoc DFT techniques
  - Add internal test points (usually multiplexers) for
    - Controllability
    - Observability
  - Added on a case-by-case basis
    - Primarily targets “hard to test” portions of chip

BASIC CONCEPTS

- Scan design
  - Transforms flip-flops of chip into a shift register
  - Scan mode facilitates
    - Shifting in test vectors
    - Shifting out responses
- Good CAD tool support
  - Transforming flip-flops to shift register
  - ATPG





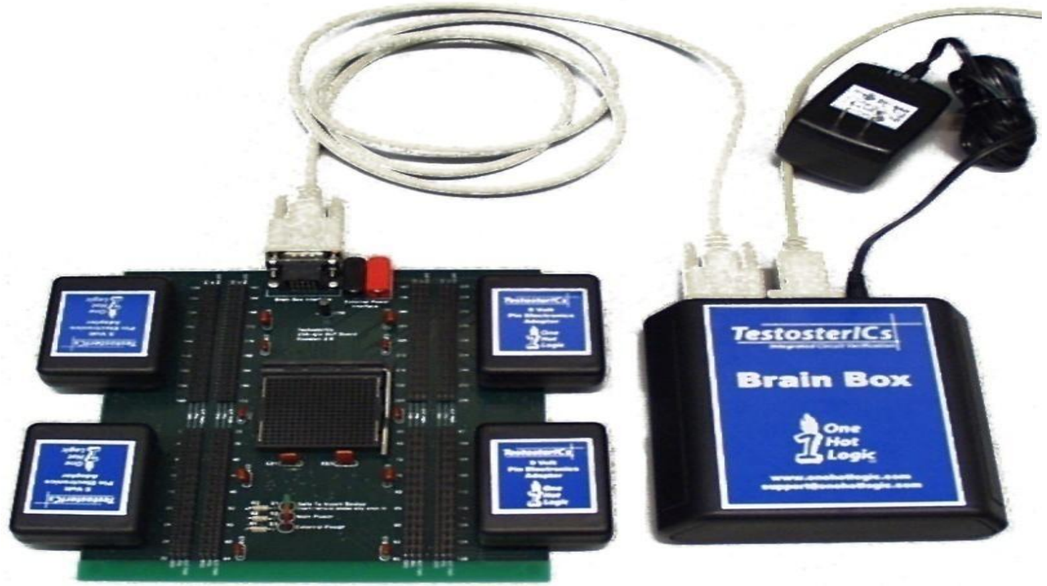


TESTING YOUR CHIP

If you don’t have a multimillion dollar tester:

Build a breadboard with LED’s and switches

Hook up a logic analyzer and pattern generator Or use a low-cost functional chip tester

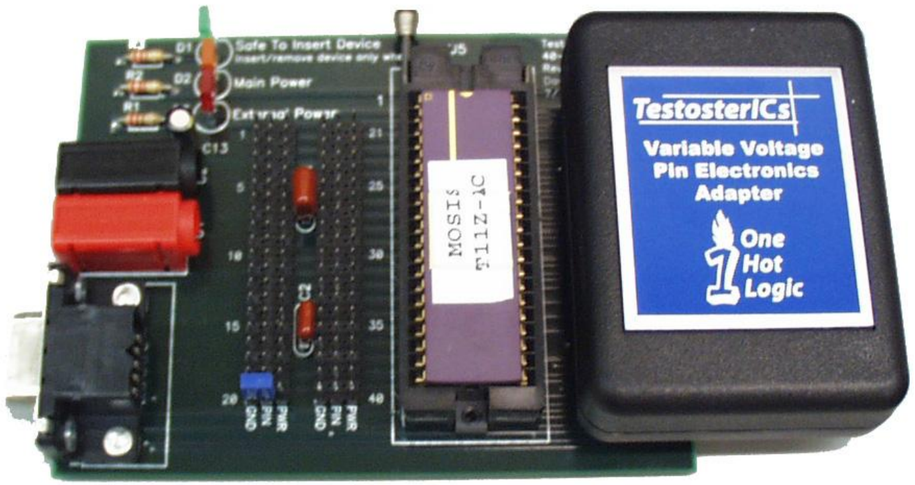


TESTING YOUR CHIP

Ex: Testoster ICs functional chip tester

Designed by clinic teams and David Diaz at HMC

Reads your IRSIM test vectors, applies them to your chip, and reports assertion failures



ASSESSMENT

1.List out Boundary scan principles & Operation modes

2. Describe about System-level testing

3.How can you do Chip level testing

SUMMARY & THANK YOU