Topic 2.7 : FET Amplifiers-Small signal analysis of CS amplifier with fixed bias.

JFET Amplifiers

* It provide an excellent voltage gain (Av) with the added advantage of a high Input Impedance (Zi).
* For this reason JFETs are often preferred over BJTs for certain types of applications.
* There are 3 basic configurations ∴ 2 Mark
  1. Common Source
  2. Common Drain (source follower)
  3. Common Gate
* The difference between BJT & JFET configurations :

BJT	JFET
It controls large output current (I_c) by means of a relative small input current (I_b).	It controls large output current (I_D) by means of a small input voltage (V_g)

Small Signal Analysis of JFET Amplifiers

* The Drain to Source current of JFET is controlled by gate to source voltage.
* The change in the drain current due to change in gate to source voltage can be determined using the transconductance factor gm.

$$g_m = \frac{\Delta I_d}{\Delta V_{GS}}$$

* Another important parameter is drain resistance r_d.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \Big|_{V_{GS} = \text{constant}}$$

AC Equivalent Circuit :-

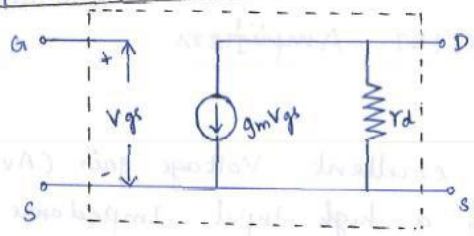

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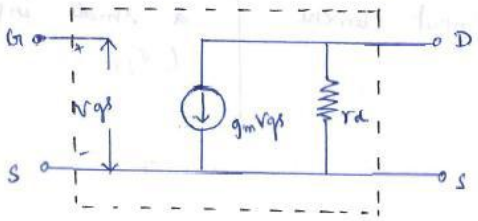
Fig: N-channel JFET- CS

* The relation of $\frac{Id}{Vgs}$ is included as current source $g_m V_{gs}$ connected from drain to source.
* The input impedance is represented by the open circuit at it's input terminal, since I_{in} is zero.
* The Output impedance is represented by rd from drain to source

Approximate AC Equivalent circuit :-

* When the value of external drain resistance R_D is very small as compared to the value of output impedance represented by rd, it's possible to replace rd by open circuit.



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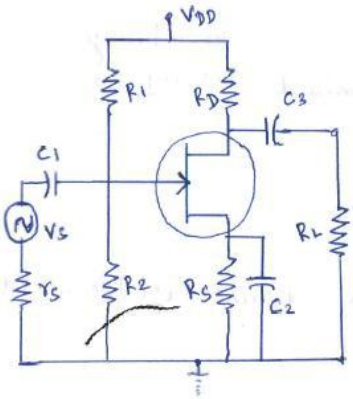
1. Common Source Circuit Analysis



=> * The input terminals are the Gate & Source, & the Output terminals are the Drain & the Source.

* So the Source terminal is common to both input & output, & the circuit configuration is known as common Source (CS

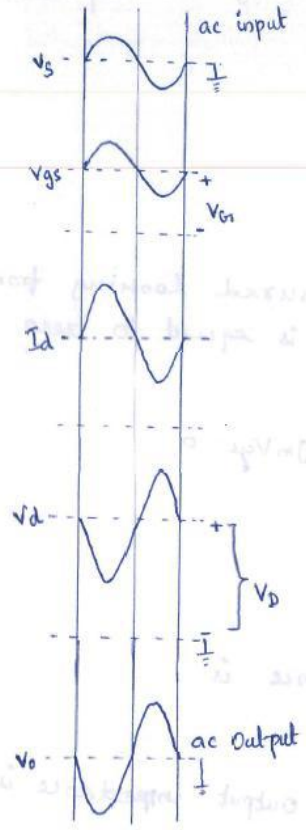


Fig: Voltage & current Waveforms

* For positive-going input signal (V_s) there is a 180° phase shift between the input & the output.
* An increase in V_s increasing the V_{GS} thus raising the level of I_D & increasing the voltage drop across R_D.
* This produces a decreases in the level of V_D, which is capacitor coupled to the circuit output as a negative going ac output voltage (V_o)
* Consequently, as V_s increases in a positive direction, V_o changes in negative direction.
* Consequently, when V_s changes in negative direction, the resultant decrease in V_{GS} reduces I_D & produces a positive-going Output.

1. JFET with Fixed Bias

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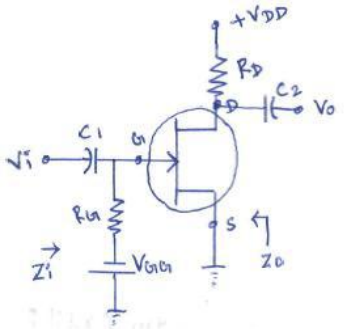
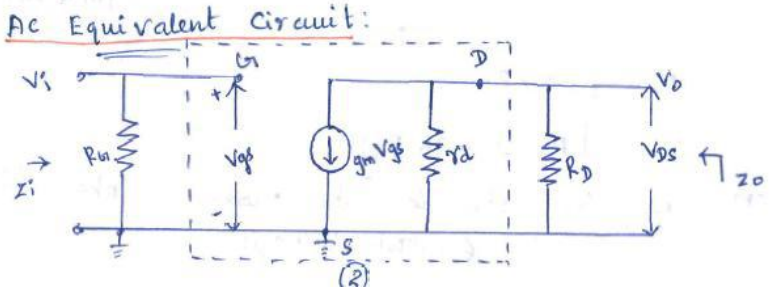


* The coupling capacitors C_1 & C_2 which are used to isolate the d.c biasing from the applied a.c signal act as short circuits for the ac analysis.

Ac Equivalent Circuit:



(2)

* The circuit is drawn by replacing all capacitors & d.c supply voltage with short circuits.

1. Input Impedance (Z_i)

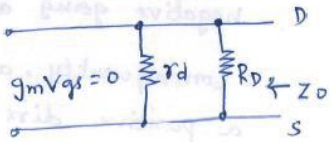
$$\boxed{Z_i = R_G}$$

2. Output Impedance (Z_o)

* It's the impedance measured looking from the output side with input voltage (V_i) is equal to zero.

* As $V_i = 0$

$V_{gs} = 0$ & hence $g_m V_{gs} = 0$



So the Output Impedance is

$$\boxed{Z_o = R_D \| r_d}$$

* if $r_d >> R_D$ Then the output impedance is

$$\boxed{Z_o \simeq R_D}$$

3. Voltage Gain (A_V)

$$A_V = \frac{V_{ds}}{V_{gs}} = \frac{V_o}{V_i}$$

$$V_o = -g_m V_{gs} (r_d \| R_D)$$

* W.K.T $V_i = V_{gs}$ Then

$$V_o = -g_m V_i (r_d \| R_D)$$

So

$$A_V = \frac{-g_m V_i (r_d \| R_D)}{V_i} = \boxed{-g_m (r_d \| R_D)}$$

* if $r_d >> R_D$

$$\boxed{A_V \simeq -g_m R_D}$$

* The negative sign indicate there is a phase shift of 180° between the input & output voltages.