SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)

COIMBATORE-35

Accredited by NBA-AICTE and Accredited by NAAC – UGC with A++ Grade

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23EET202 / DIGITAL ELECTRONICS AND INTEGRATED CIRCUITS

II YEAR / III SEMESTER

UNIT-II: DESIGN OF COMBINATIONAL AND SEQUENTIAL CIRCUITS

FLIP FLOPS – SR, D

Dr.R.Senthil Kumar

TOPIC OUTLINE

Memory devices

RS Flip Flop

D Flip Flop

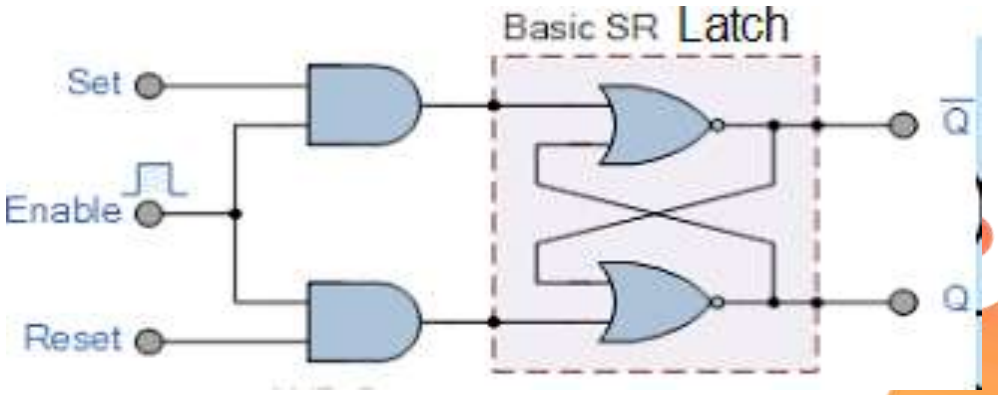
IC Devices

Recap

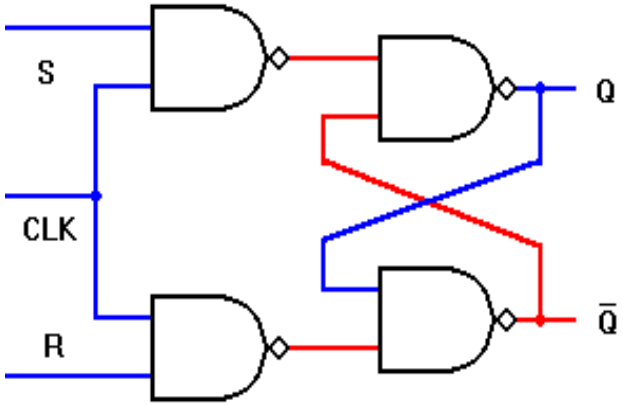
RS FLIP FLOP

RS Flip Flop

- The RS flip flop is the basic memory element with clock input as enable point **(Clocked RS Latch)**
- Two input signals, S - set and R - signal.
- E - clock signal acting as enable.



RS Flip Flop – Circuit, Truth table

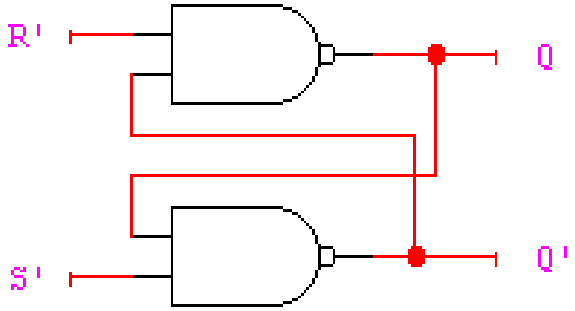


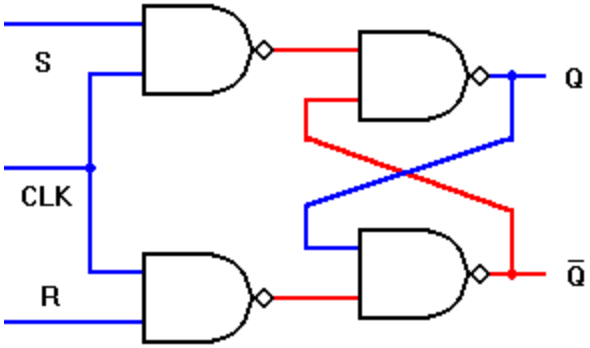
S	*R*	*Q*	*Q'*
0	0	1	0
0	1	0	1
1	0	1	0
1	1	?	?

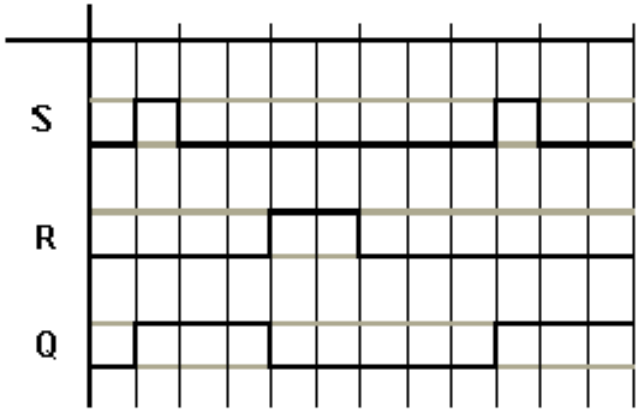
RS Flip-Flop - Characteristics table

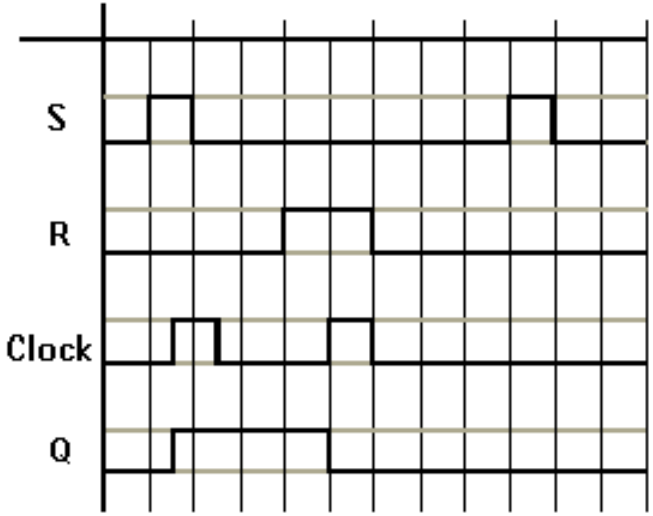
C	*S*	*R*	*Q*(*t*)	*Q*(*t*+1)	
0	X	X	0	0	No change
0	X	X	1	1	
1	0	0	0	0	No change
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	?	Forbidden
1	1	1	1	?	

RS Latch / RS Flip Flop









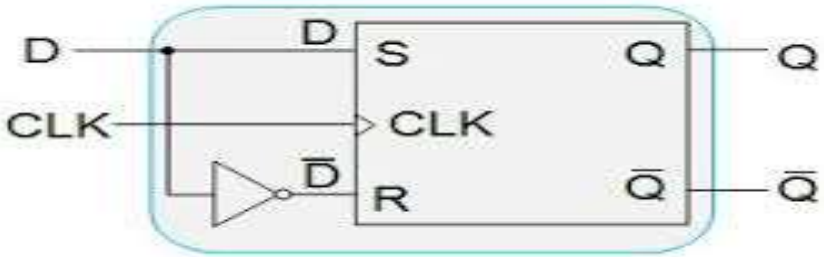
Latch

Flip-flop

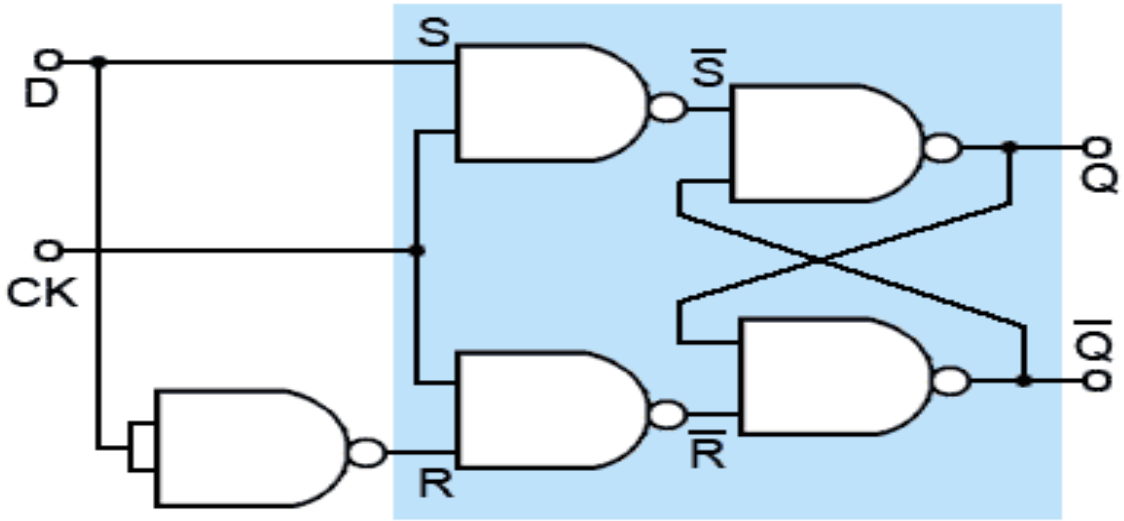
D FLIP FLOP

D Flip flop

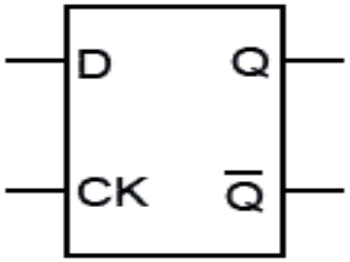
- The D stands for “Data” or “Delay” Flip flop
- It has one input signal, D which is set when it is “1” and reset when it is “0”
- The demerit of SR flip flop is forbidden value, ie the input - S & R is ‘1”. It is over comed here.



D Flip-Flop: Circuit, block, truth table



Inputs		Outputs	
CK	D	Q	$\overline{Q}$
0	X	No change	
1	0	0	1
1	1	1	0



D Flip-Flop: Ch. table

C	*D*	*Q*(*t*)	*Q*(*t*+1)	
0	X	0	0	No change
0	X	1	1	
1	0	0	0	Reset
1	0	1	0	
1	1	0	1	Set (Data)
1	1	1	1	

LATCH / FLIP-FLOP DEVICES

Device	# of Elements	Description
74LS73A	2	Negative-edge triggered JK flip-flop with clear
7474	2	Positive-edge triggered D flip-flop with preset and clear
74LS75	4	D Latch with enable
7476	2	Pulse-edge triggered JK flip-flop with preset and clear
74111	2	Master-slave JK flip-flop with preset, clear, and data lock out
74116	2	4-bit hazard-free D latch with clear and dual enable
74175	4	Positive-edge triggered D flip-flop with clear
74273	8	Positive-edge triggered D flip-flop with clear
74276	4	Negative-edge triggered JK flip-flop with preset and clear
74279	4	SR latch with active-low inputs

SUMMARIZE

…A CASE STUDY & THANK YOU