SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)

COIMBATORE-35

Accredited by NBA-AICTE and Accredited by NAAC – UGC with A++ Grade

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

23EET202 / DIGITAL ELECTRONICS AND INTEGRATED CIRCUITS

II YEAR / III SEMESTER

UNIT-II: DESIGN OF COMBINATIONAL AND SEQUENTIAL CIRCUITS

FLIP FLOPS – JK,T

TOPIC OUTLINE

JK Flip Flop

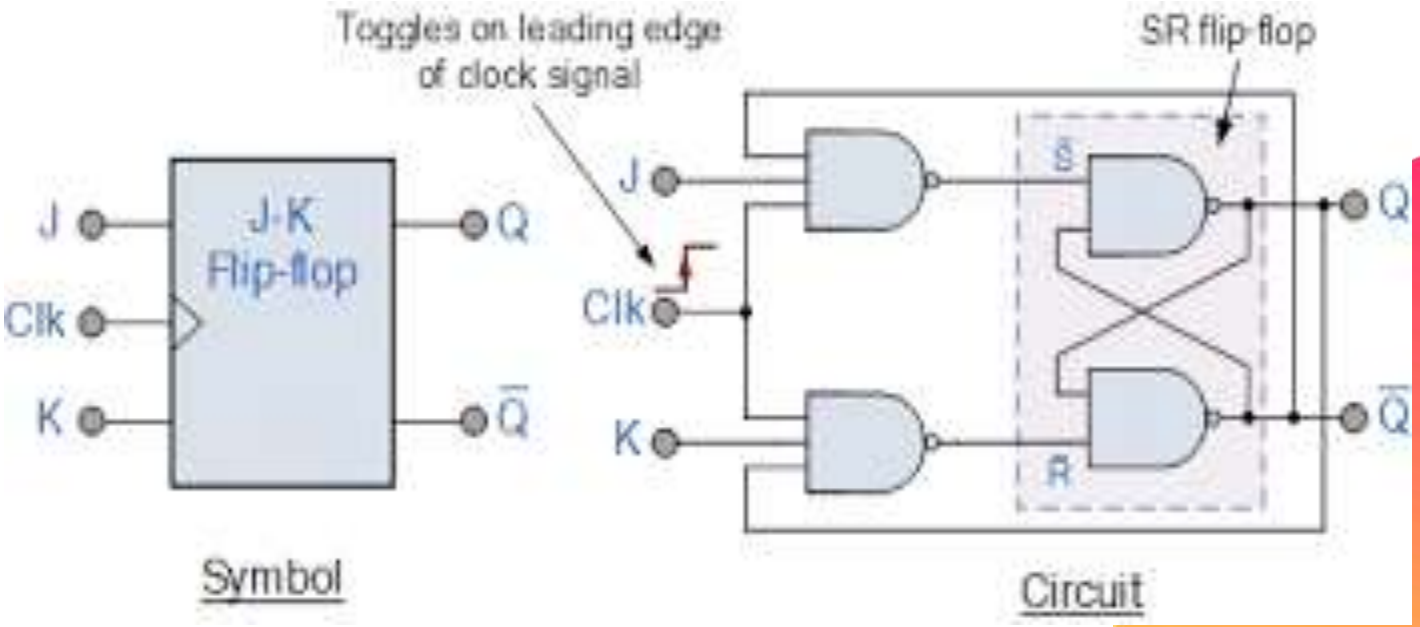
T Flip Flop

Triggering pulses

Recap

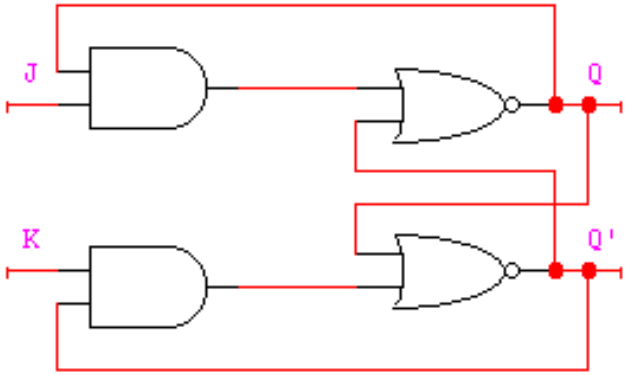
JK FLIP FLOP

- The JK flip flop consist of two RS flip flop
- Two input signals, J - set and K - reset
- SR = 1, forbidden is over come with next change



JK Ch. Table and equation

J	*K*	*Q*(*n*)	*Q*(*n*+1)	
0	0	0	0	Hold
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	1	Toggle
1	1	1	0	

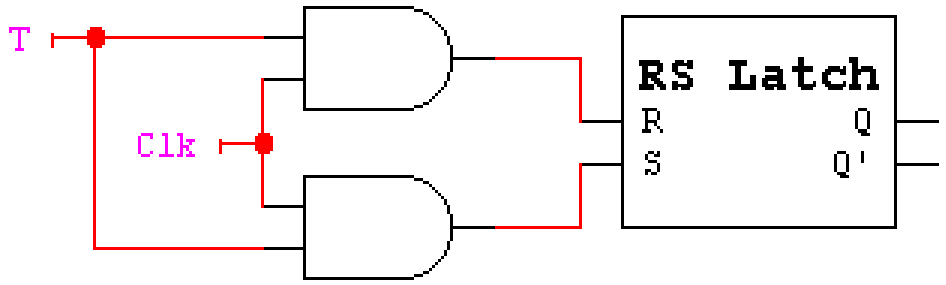


Ch. equation:

$Q^+ = K'Q + JQ'$

T (TOGGLE) FLIP-FLOP

T	*Q*(*n*)	*Q*(*n*+1)	
0	0	0	Hold
0	1	1	
1	0	1	Toggle
1	1	0	

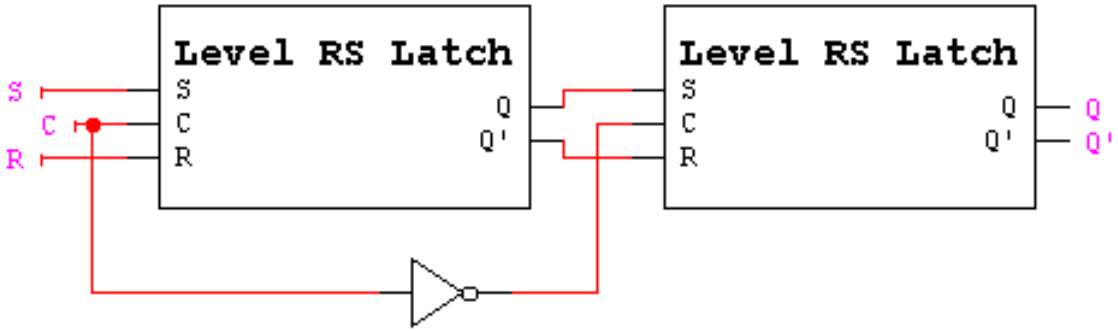


Ch. Eqn: $Q^+ = TQ' + T'Q$

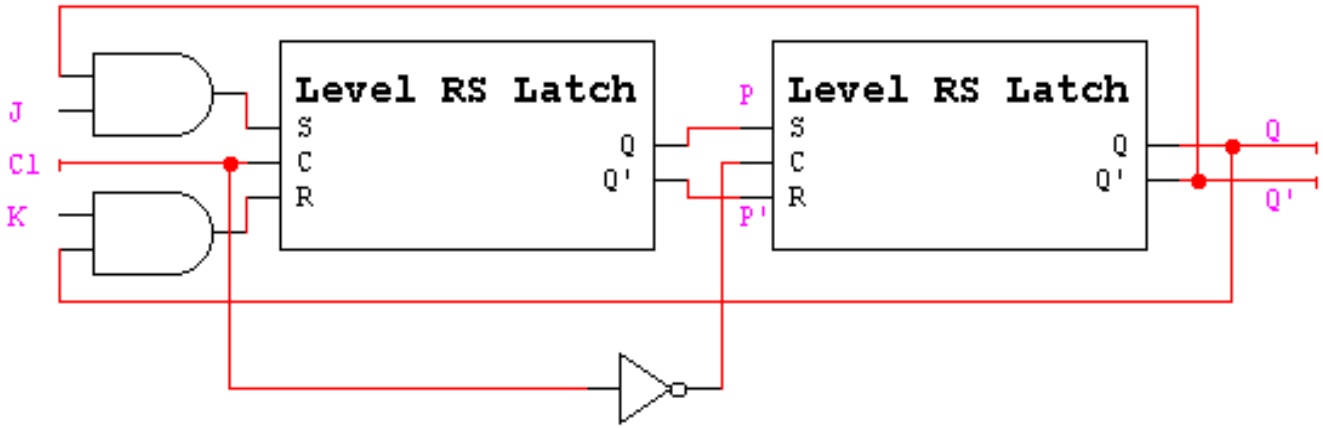
MASTER SLAVE FLIP-FLOPS

A *master slave flip-flop* consists of two latches and an inverter.

Master-slave RS flip-flop



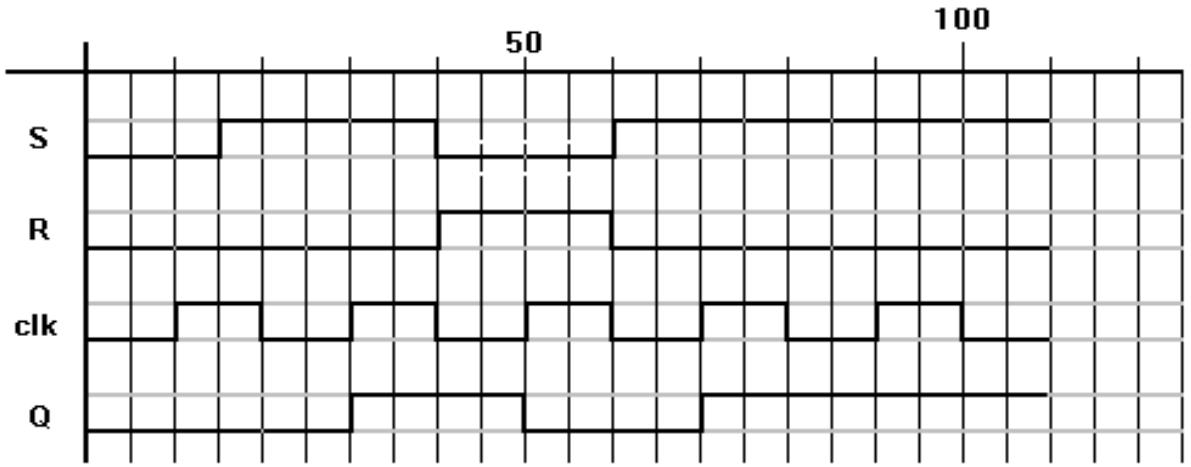
Master-Slave JK Flip-Flops



TRIGGERING PULSES

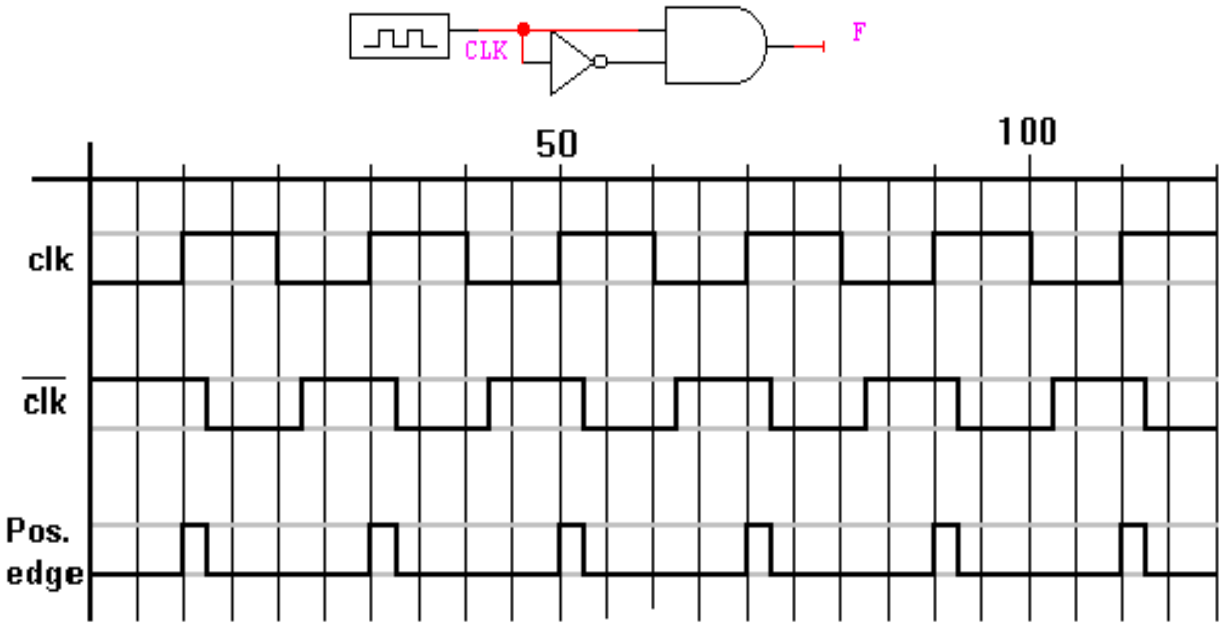
Positive edge-triggered RS flip-flop timing diagram.

(The opposite is negative edge triggered)



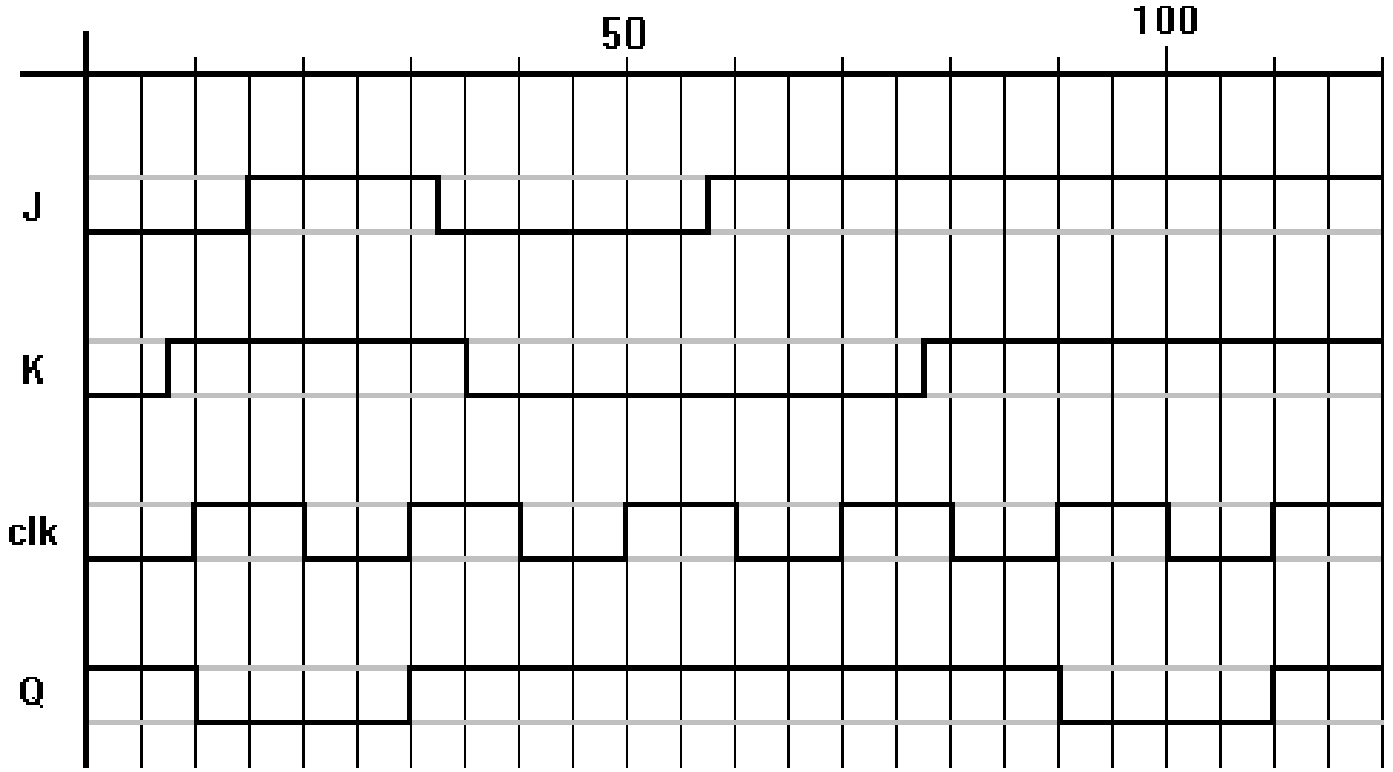
Positive Edge-Triggered Timing

A circuit that generates a positive edge-triggered timing signal can be constructed as follows:



TRIGGERING PULSES

Positive edge-triggered JK flip-flop timing diagram



Edge / Level-Triggered Timing

Type	When inputs are sampled	When outputs are valid
Unclocked latch	Always	Propagation delay from input change
Level-sensitive latch	Clock high	Propagation delay from input change
Positive-edge latch	Clock low-to-high transition	Propagation delay from rising edge of clock
Negative-edge latch	Clock high-to-low transition	Propagation delay from falling edge of clock
Master/slave flip-flop	Clock high-to-low transition	Propagation delay from falling edge of clock

SUMMARIZE

…THANK YOU