SNS COLLEGE OF TECHNOLOGY

Coimbatore-35

An Autonomous Institution

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Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

23ECB201 – DIGITAL SYSTEM DESIGN

II YEAR/ III SEMESTER

UNIT 4 – DESIGN OF SEQUENTIAL CIRCUITS

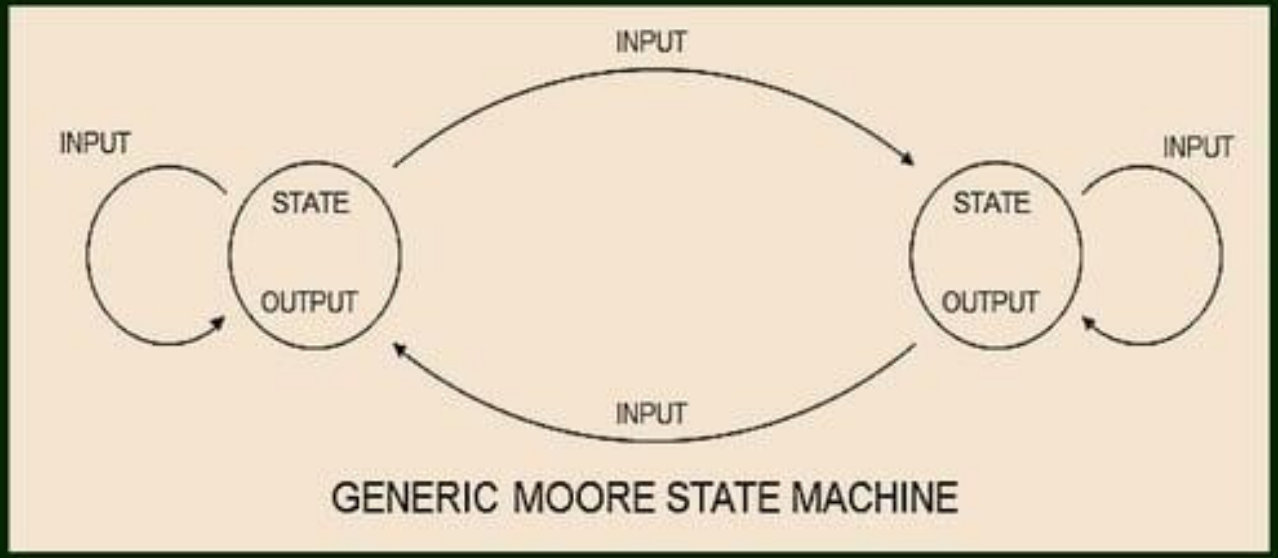
TOPIC –DESIGN OF SEQUENTIAL CIRCUITS

Finite State Machines

- Two types of sequential circuits (or finite state machines)
  - Mealy machine
    - Output is function of present state and present input
  - Moore machine
    - Output is function of present state only

Moore State Machines:

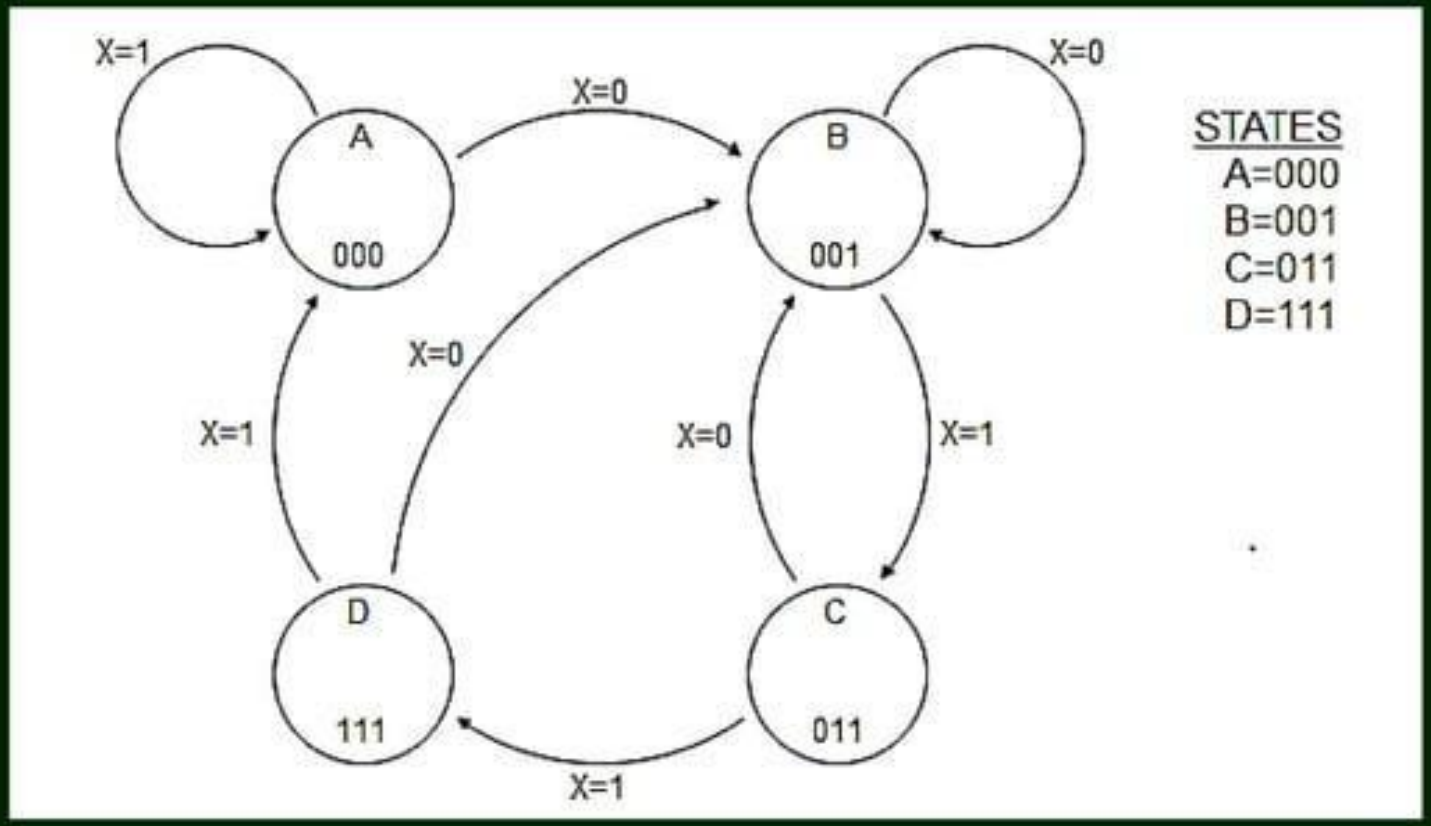
- Outputs determined solely by the current state



State Table

Prev. State	X	O_2	O_1	O_0	Next State$^+$
A	0	0	0	0	B
A	1	0	0	0	A
B	0	0	0	1	B
B	1	0	0	1	C
D	0	1	1	1	B
D	1	1	1	1	A
C	0	0	1	1	B
C	1	0	1	1	D

State Diagram



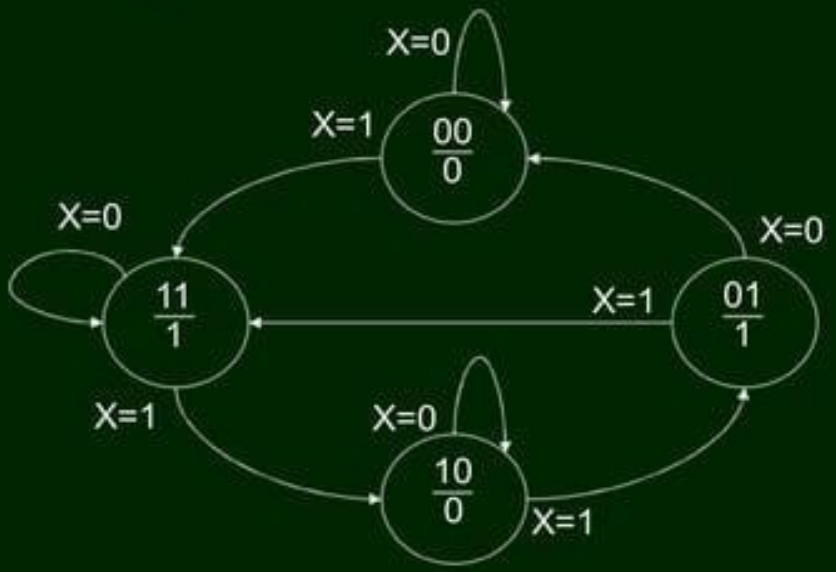
Moore State Machines:

- State Table

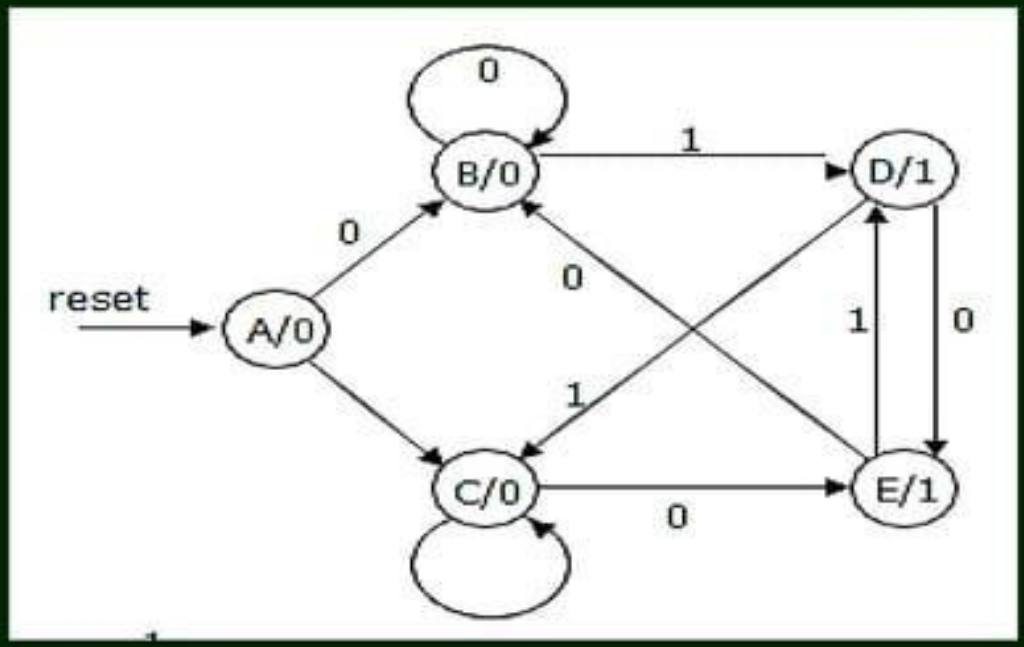
	NS		
PS	X=0	X=1	
AB	AB	AB	z (=B)
00	00	11	0
01	00	11	1
10	10	01	0
11	11	10	1

Moore State Machines:

- State Diagram



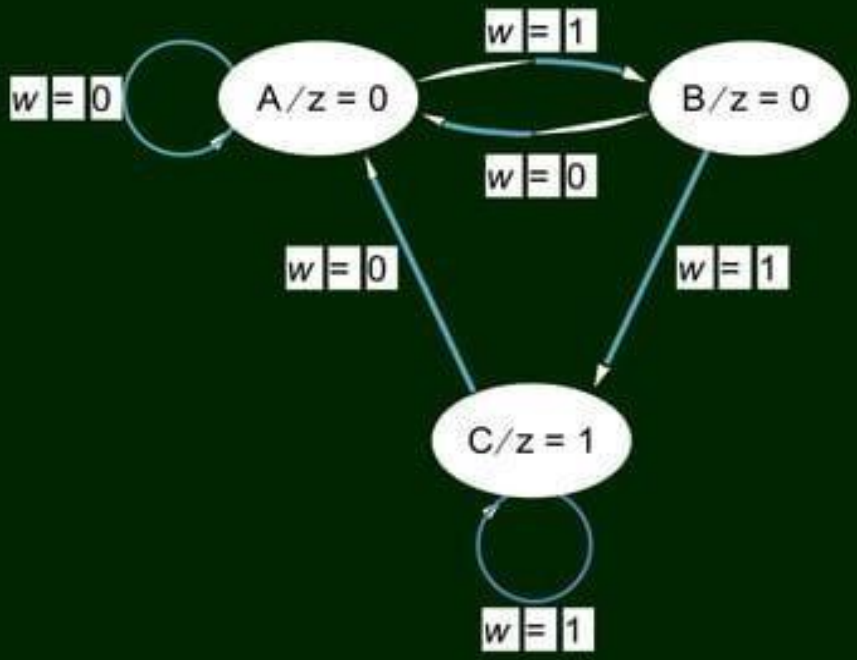
Moore Machine



Moore Machine

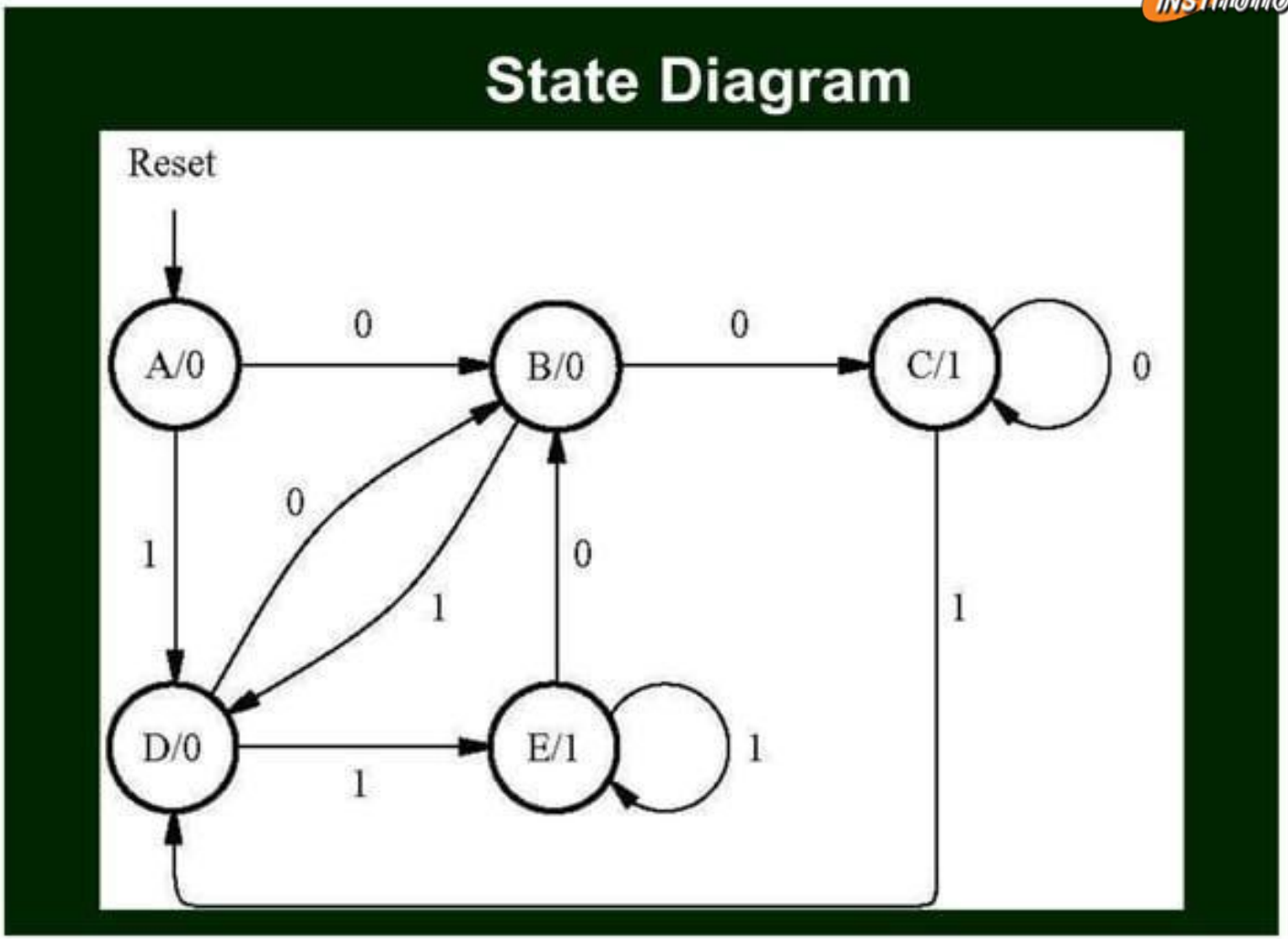
reset	input	current state	next state	output
1	—	—	A	
0	0	A	B	0
0	1	A	C	0
0	0	B	B	0
0	1	B	D	0
0	0	C	E	0
0	1	C	C	0
0	0	D	E	1
0	1	D	C	1
0	0	E	B	1
0	1	E	D	1

Moore FSM – Example : State diagram



Moore FSM – Example : State table

Present state	Next state $w = 0$	Next state $w = 1$	Output z
A	A	B	0
B	A	C	0
C	A	C	1

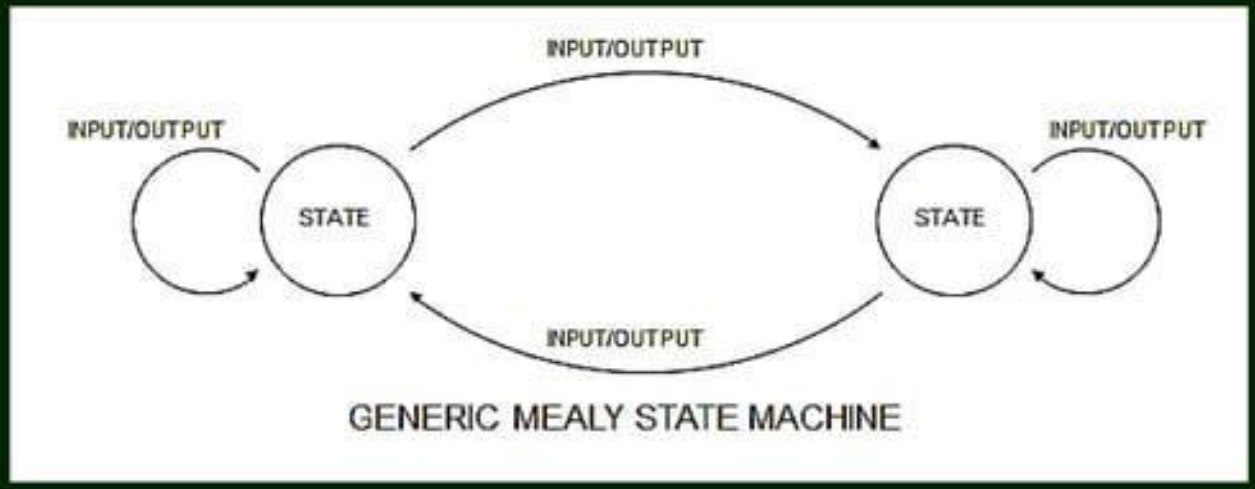

State Diagram
Reset
A/0
B/0
C/1
D/0
E/1
0
0
0
1
0
1
0
1
1
1

State Table

Present state	Next state		Output
	$w = 0$	$w = 1$	z
A	B	D	0
B	C	D	0
C	C	D	1
D	B	E	0
E	B	E	1

Mealy State Machines:

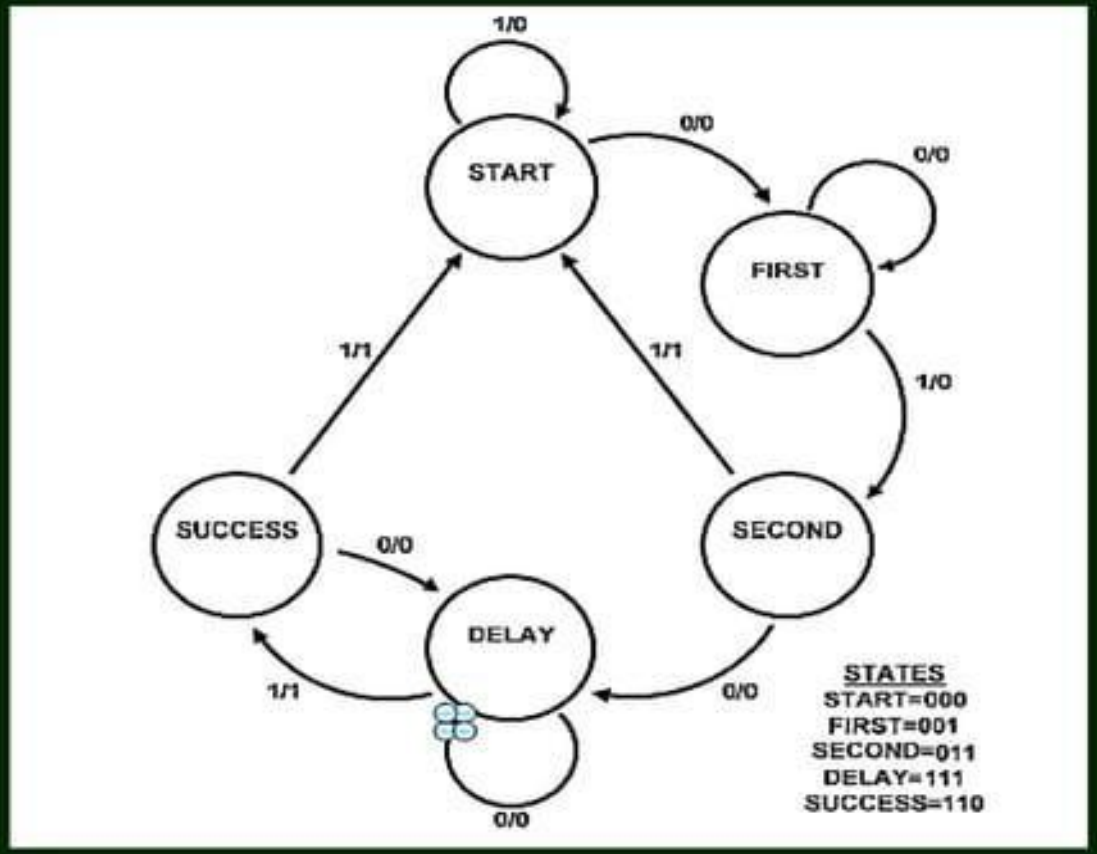
- Outputs determined by the current state and the current inputs.



GENERIC MEALY STATE MACHINE

State	Q_2	Q_1	Q_0	X	Z	State$^+$	$Q2^+$	$Q1^+$	Q
Start	0	0	0	0	0	First	0	0	1
Start	0	0	0	1	0	Start	0	0	0
First	0	0	1	0	0	First	0	0	1
First	0	0	1	1	0	Second	0	1	1
Success	0	1	0	0	0	First	0	0	1
Success	0	1	0	1	0	Start	0	0	0
Second	0	1	1	0	0	Delay	1	1	1
Second	0	1	1	1	1	Success	0	1	0
unused	1	0	*	*	X	X	X	X	X
SuccessD	1	1	0	0	0	Delay	1	1	1
SuccessD	1	1	0	1	1	Success	0	1	0
Delay	1	1	1	0	0	Delay	1	1	1
Delay	1	1	1	1	1	SuccessD	1	1	0

State Diagram



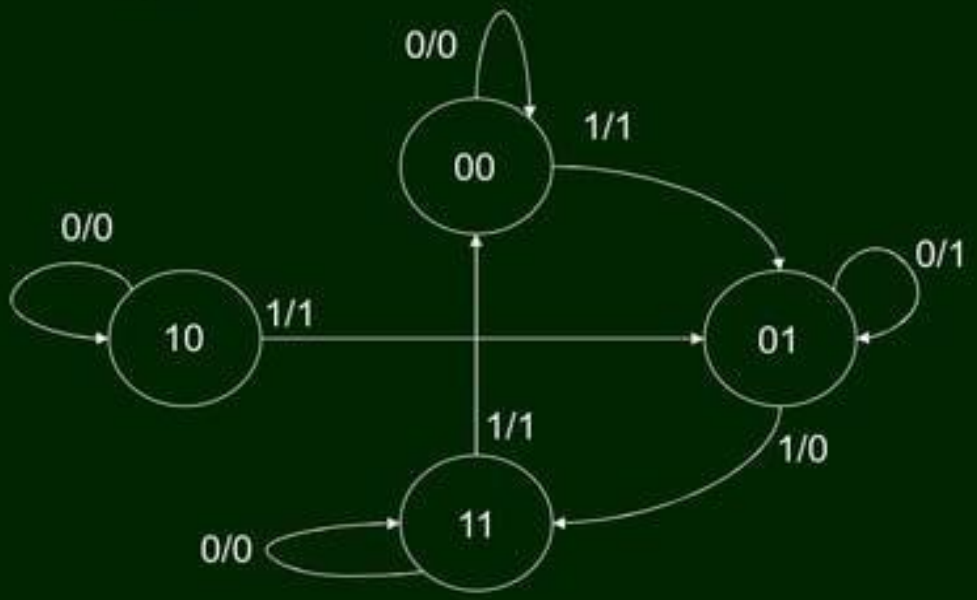
Mealy State Machines:

- State Table

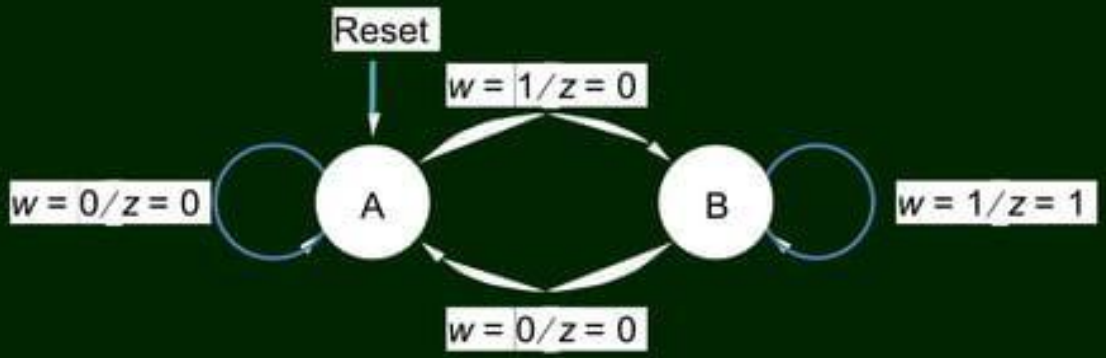
PS	NS x=0	NS x=1
AB	AB,z	AB,z
00	00,0	01,1
01	01,1	11,0
10	10,0	01,1
11	11,0	00,1

Mealy State Machines:

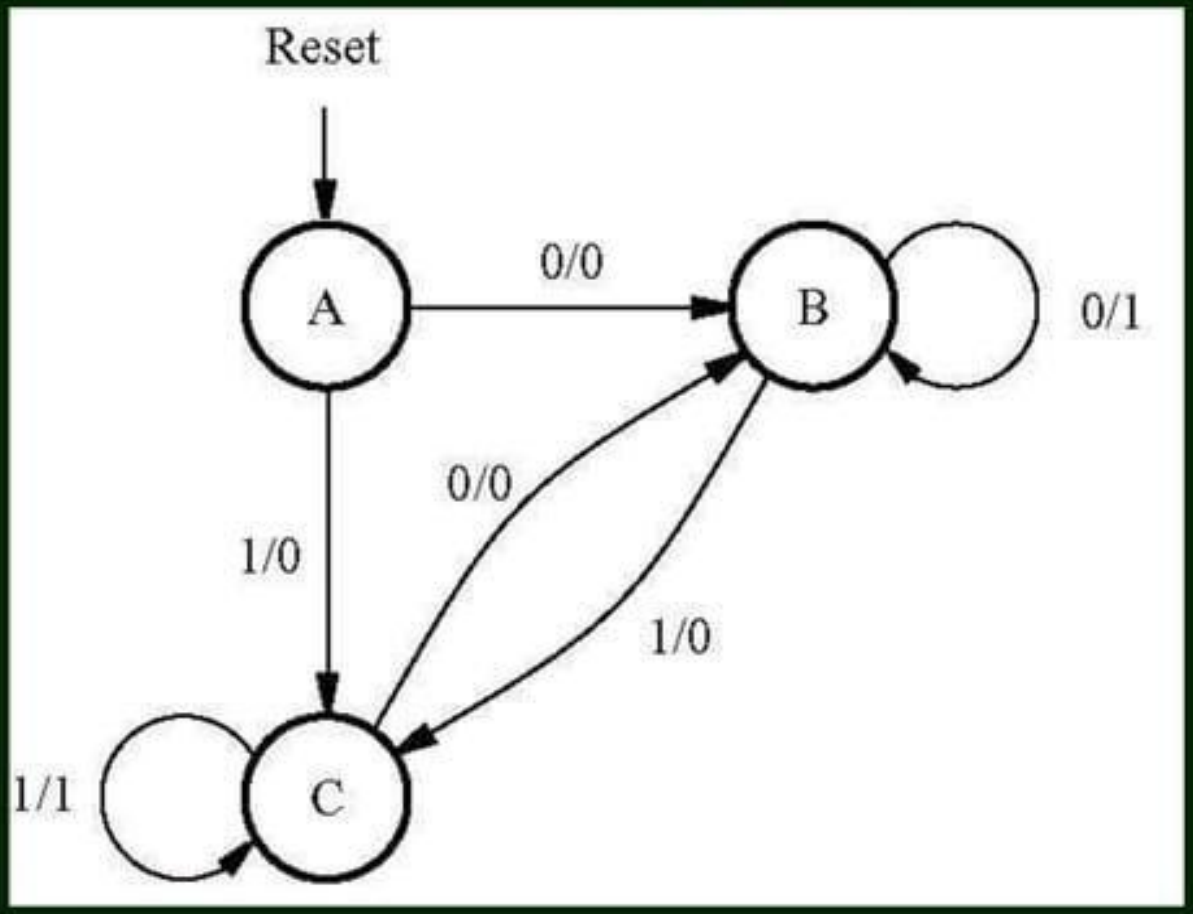
- State Diagram



Mealy FSM – Example : State diagram



State Diagram



State Table

Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	B	C	0	0
B	B	C	1	0
C	B	C	0	1

THANK YOU