SNS COLLEGE OF TECHNOLOGY

Coimbatore-35

An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A++' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

23ECB201 – DIGITAL SYSTEM DESIGN

II YEAR/ III SEMESTER

UNIT 4 – SHIFT REGISTERS AND COUNTERS

TOPIC –REGISTERS,SHIFT REGISTERS

REGISTERS

- A **register** is basically a storage space for units of memory that are used to transfer data for immediate use by the CPU (Central Processing Unit) for data processing.
- Also known as memory registers, they can actually form part of the computer processor as a processor register.
- The register is large enough to hold any kind of data, such as dates, instruction sets, storage addresses, bits, sequences, and characters.

- Some instruction sets are partly formed by registers.
- Types of registers include memory address register, memory buffer register, input output address register, input output buffer register, and shift register.

Shift Register

- One flip-flop can store one-bit of information.
- In order to store multiple bits of information, we require multiple flip-flops.
- The group of flip-flops, which are used to hold and store the binary data is known as **register**.
- If the register is capable of shifting bits either towards right hand side or towards left hand side is known as **shift register**.

Types of Shift Register

The types of shift registers based on applying inputs and accessing of outputs.

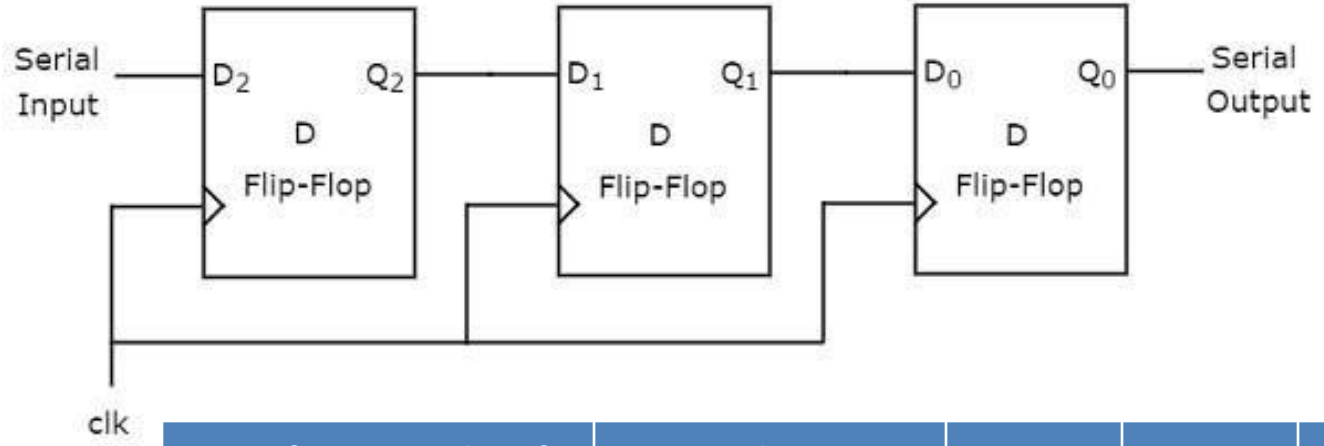
- Serial In – Serial Out shift register
- Serial In – Parallel Out shift register
- Parallel In – Serial Out shift register
- Parallel In – Parallel Out shift register
- Bidirectional shift register
- Universal shift register

Serial In – Serial Out shift register (SISO)

- The shift register, which allows serial input and produces serial output is known as Serial In – Serial Out shift register.
- The circuit diagram consists of three D flip-flops, which are **cascaded**. The output of one D flip-flop is connected as the input of next D flip-flop. All these flip-flops are synchronous with each other since, the same clock signal is applied to each one.

- In this shift register, the bits can be sent serially from the input of left most D flip-flop. Hence, this input is also called as **serial input**.
- For every positive edge triggering of clock signal, the data shifts from one stage to the next. So, we can receive the bits serially from the output of right most D flip-flop. Hence, this output is also called as **serial output**.

Serial In – Serial Out shift register (SISO)



No of positive edge of Clock	Serial Input	Q_2	Q_1	Q_0
0	-	0	0	0
1	1LSB	1	0	0
2	1	1	1	0
3	0MSB	0	1	1 LSB
4	-	-	0	1
5	-	-	-	0 MSB

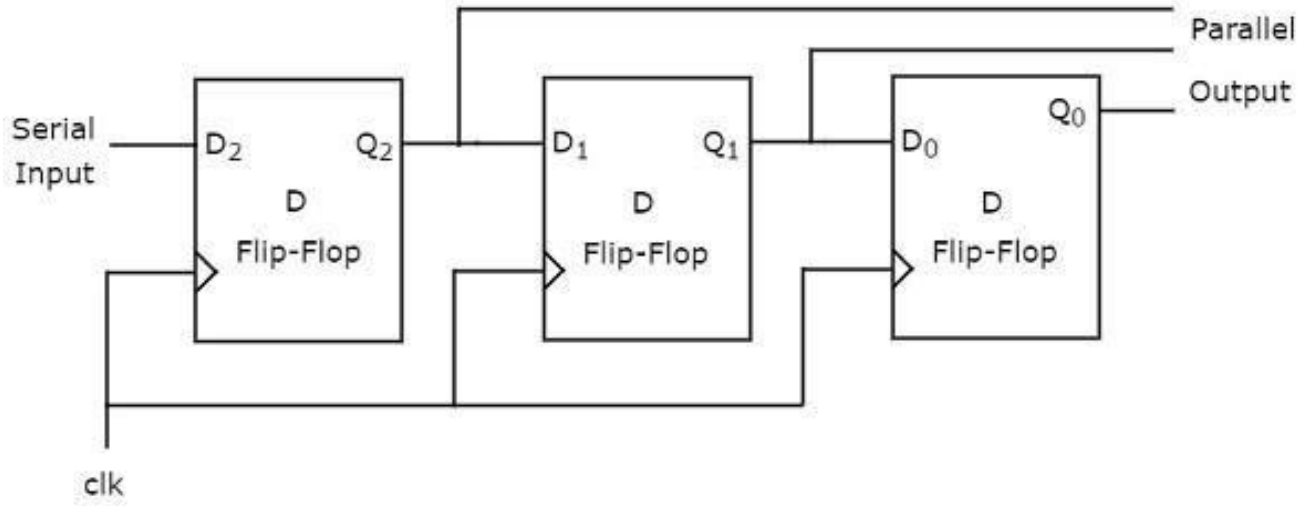
Serial In - Parallel Out Shift Register

- The shift register, which allows serial input and produces parallel output is known as Serial In – Parallel Out SIPO shift register.
- This circuit consists of three D flip-flops, which are cascaded. The output of one D flip-flop is connected as the input of next D flip-flop. All these flip-flops are synchronous with each other since.

- In this shift register, the bits can be sent serially from the input of left most D flip-flop. Hence, this input is also called as **serial input**.
- For ev ery positive edge triggering of clock signal, the data shifts from one stage to the next. In this case, we can access the outputs of each D flip-flop in parallel.

So, will get **parallel outputs** from this shift register.

Serial In - Parallel Out Shift Register



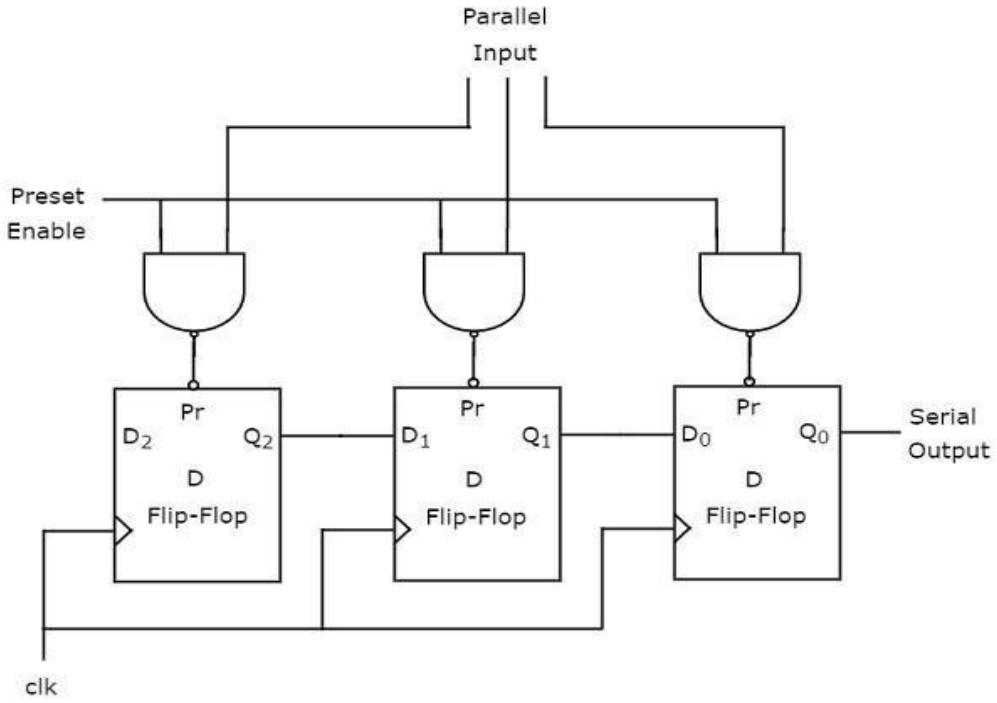
No of positive edge of Clock	Serial Input	Q_2 MSB	Q_1	Q_0 LSB
0	-	0	0	0
1	1LSB	1	0	0
2	1	1	1	0
3	0MSB	0	1	1

Parallel In – Serial Out Shift Register

- The shift register, which allows parallel input and produces serial output is known as Parallel In – Serial Out PISO
- This circuit consists of three D flip-flops, which are cascaded . The output of one D flip-flop is connected as the input of next D flip-flop.
- All these flip-flops are synchronous with each other since, the same clock signal is applied to each one.

- In this shift register, we can apply the **parallel inputs** to each D flip-flop by making Preset Enable to 1.
- For every positive edge triggering of clock signal, the data shifts from one stage to the next. So, we will get the **serial output** from the right most D flip-flop.

Parallel In – Serial Out Shift Register



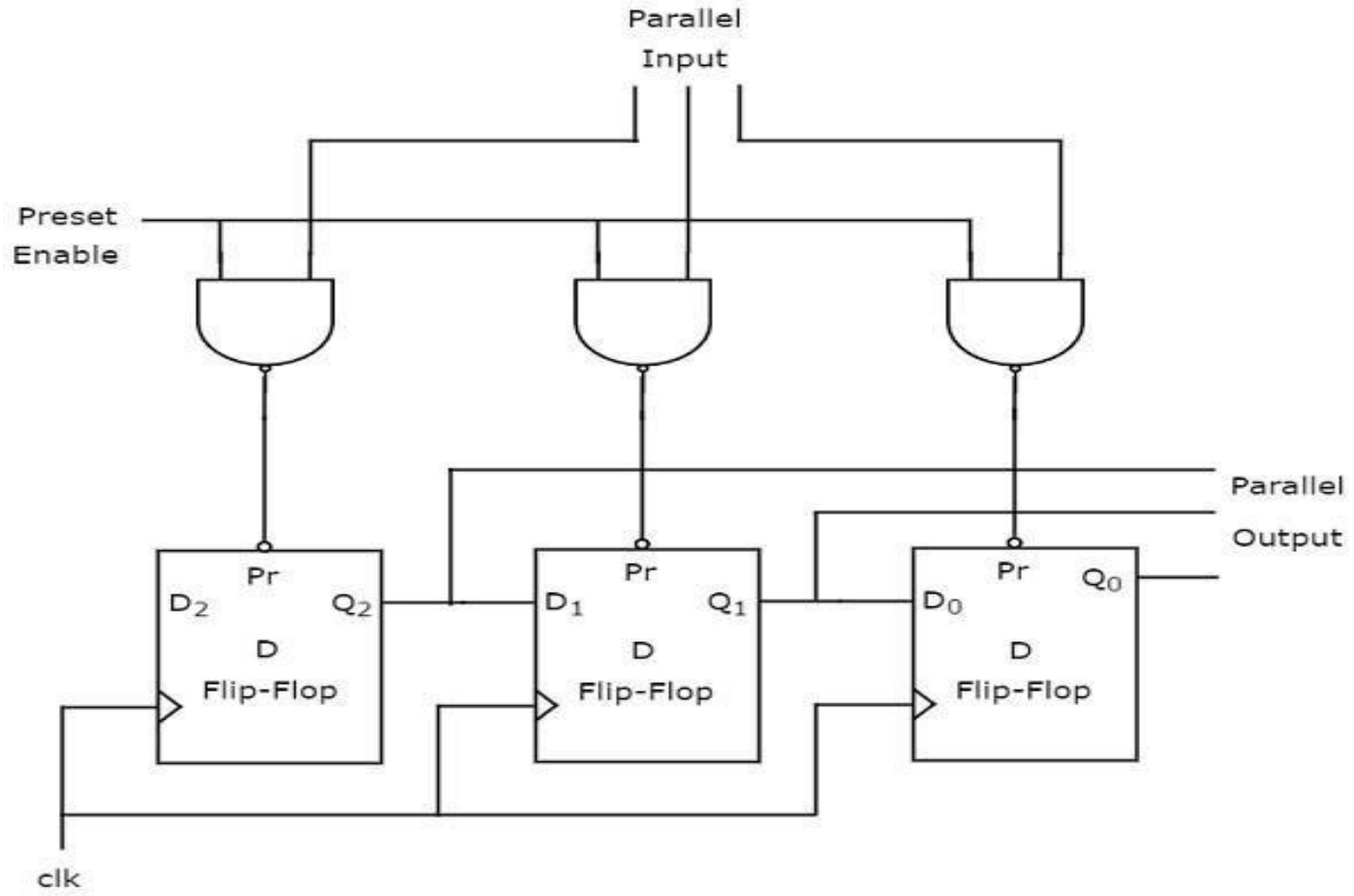
No of positive edge of Clock	Q_2	Q_1	Q_0
0	0	1	1LSB
1	-	0	1
2	-	-	0LSB

Parallel In - Parallel Out Shift Register

- The shift register, which allows parallel input and produces parallel output is known as Parallel In − Parallel Out PIPO shift register.
- This circuit consists of three D flip-flops, which are cascaded. The output of one D flip-flop is connected as the input of next D flip-flop. All these flip-flops are synchronous with each other since, the same clock signal is applied to each one.

- In this shift register, we can apply the **parallel inputs** to each D flip-flop by making Preset Enable to 1. We can apply the parallel inputs through preset or clear. These two are asynchronous inputs.
- The flip-flops produce the corresponding outputs, based on the values of asynchronous inputs. In this case, the effect of outputs is independent of clock transition. So, we will get the **parallel outputs** from each D flip-flop.

Parallel In - Parallel Out Shift Register



Applications of shift Registers

- The shift registers are used for temporary data storage.
- The shift registers are also used for data transfer and data manipulation.
- The serial-in serial-out and parallel-in parallel-out shift registers are used to produce time delay to digital circuits.
- The serial-in parallel-out shift register is used to convert serial data into parallel data thus they are used in communication lines where demultiplexing of a data line into several parallel line is required.
- AParallel in Serial out shift register us used to convert parallel data to serial data.

THANK YOU