

SNS COLLEGE OF TECHNOLOGY

Coimbatore-35 An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A++' Grade Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

2 3ECB201 – DIGITAL SYSTEMS DESIGN

II YEAR/ III SEMESTER

UNIT 3 – SEQUENTIAL CIRCUITS

TOPIC 3.5&6 - Analysis and design of clocked sequential

circuits - Finite State Machines - Mealy Model







Analysis and design of clocked sequential circuits

Sequential circuit

- > A logic diagram is recognized as a clocked sequential circuit if it includes flip-flops with clock inputs
- >The flip-flops may be of any type, and the logic diagram may or may not include combinational logic gates





Analysis and design of clocked sequential circuits - Finite State Machines - Mealy Model

STATE TABLE and STATE Diagram * State diagreen and State tuble are both ways to represent the relationship between imputs, outputs, Present States, and next States of a Sequential circuit. ANTAN 9I x Ra Pri stor B 6B PB Taz z 68 Menly CIK 9-1-13 LA trait Analysis of clucked Segnenhint cut

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JTATE EQUATION / TRANSITION EQUATION A (E+1) = AX+BZ B (E+1) = AX Output Equation y = (A+B)x STATE TABLE OF TRANSITION TABLE output A B purios in put 1 A-B 0 × 0 0 0 139 1 0 0 0 1 0 12/1 0 0 0 0 10 0 0

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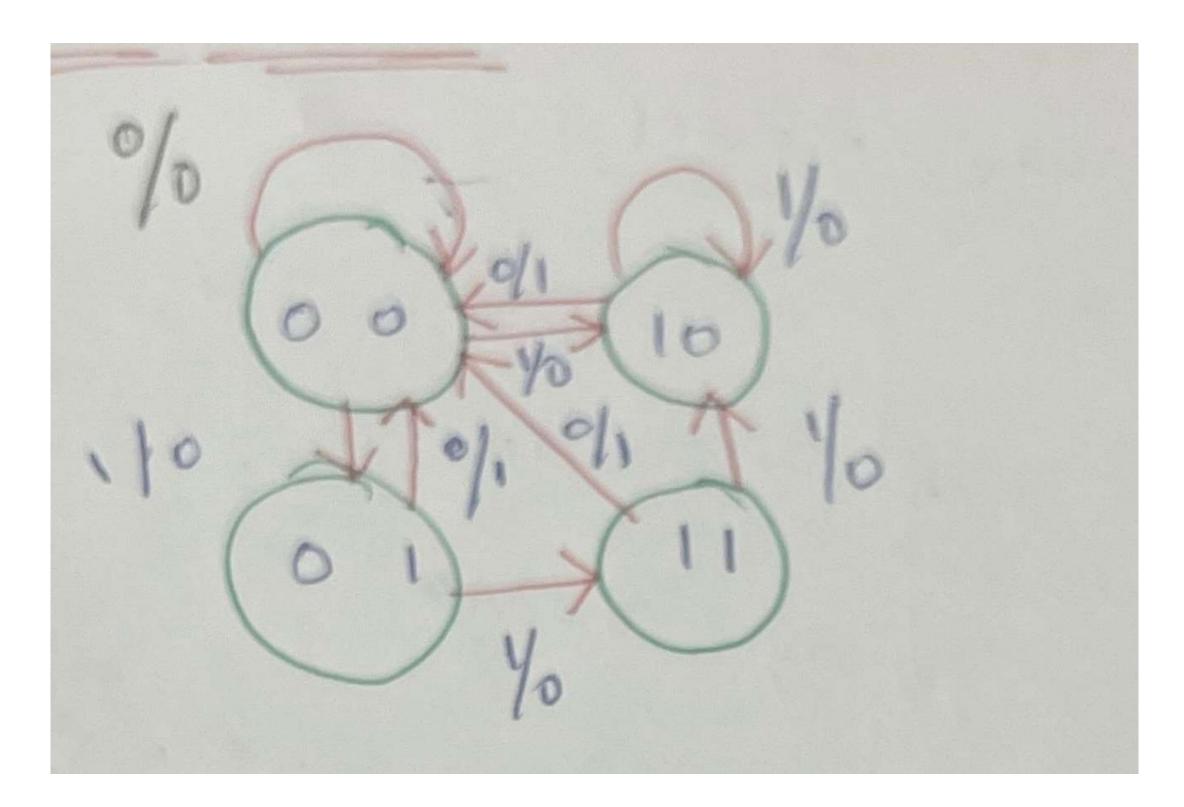
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Analysis and design of clocked sequential circuits -Finite State Machines - Mealy Model



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THANK YOU

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