



SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution



Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A++' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

2 3ECB201 – DIGITAL SYSTEMS DESIGN

II YEAR/ III SEMESTER

1

UNIT 3 – SEQUENTIAL CIRCUITS

TOPIC 3.5&6 - Analysis and design of clocked sequential
circuits - Finite State Machines - Mealy Model



Analysis and design of clocked sequential circuits

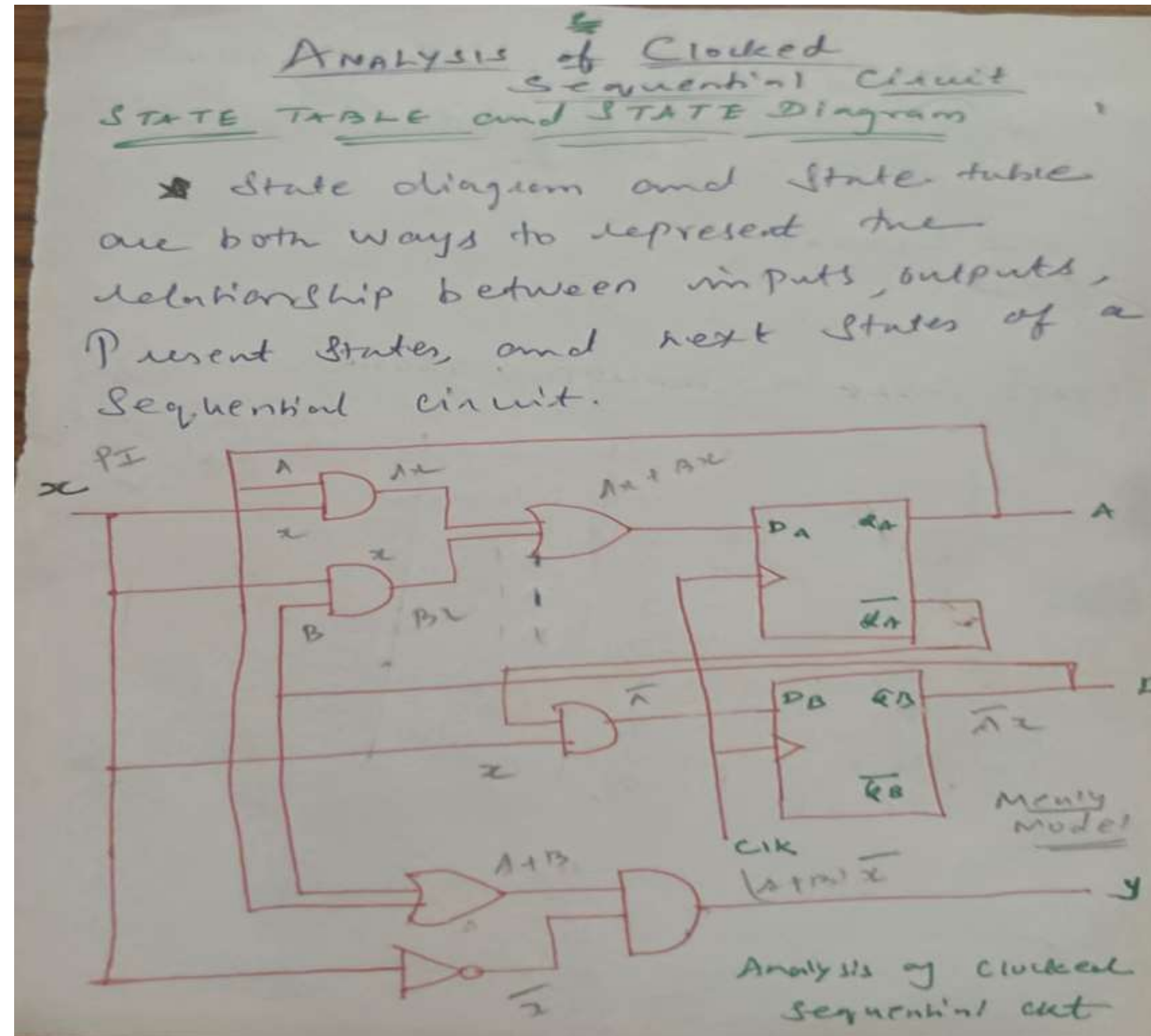


Sequential circuit

- A logic diagram is recognized as a clocked sequential circuit if it includes flip-flops with clock inputs
- The flip-flops may be of any type, and the logic diagram may or may not include combinational logic gates



Analysis and design of clocked sequential circuits - Finite State Machines - Mealy Model





Analysis and design of clocked sequential circuits - Finite State Machines - Mealy Model

STATE EQUATION / TRANSITION EQUATION

$$A(t+1) = Ax + Bx$$
$$B(t+1) = \bar{A}x$$

Output Equation

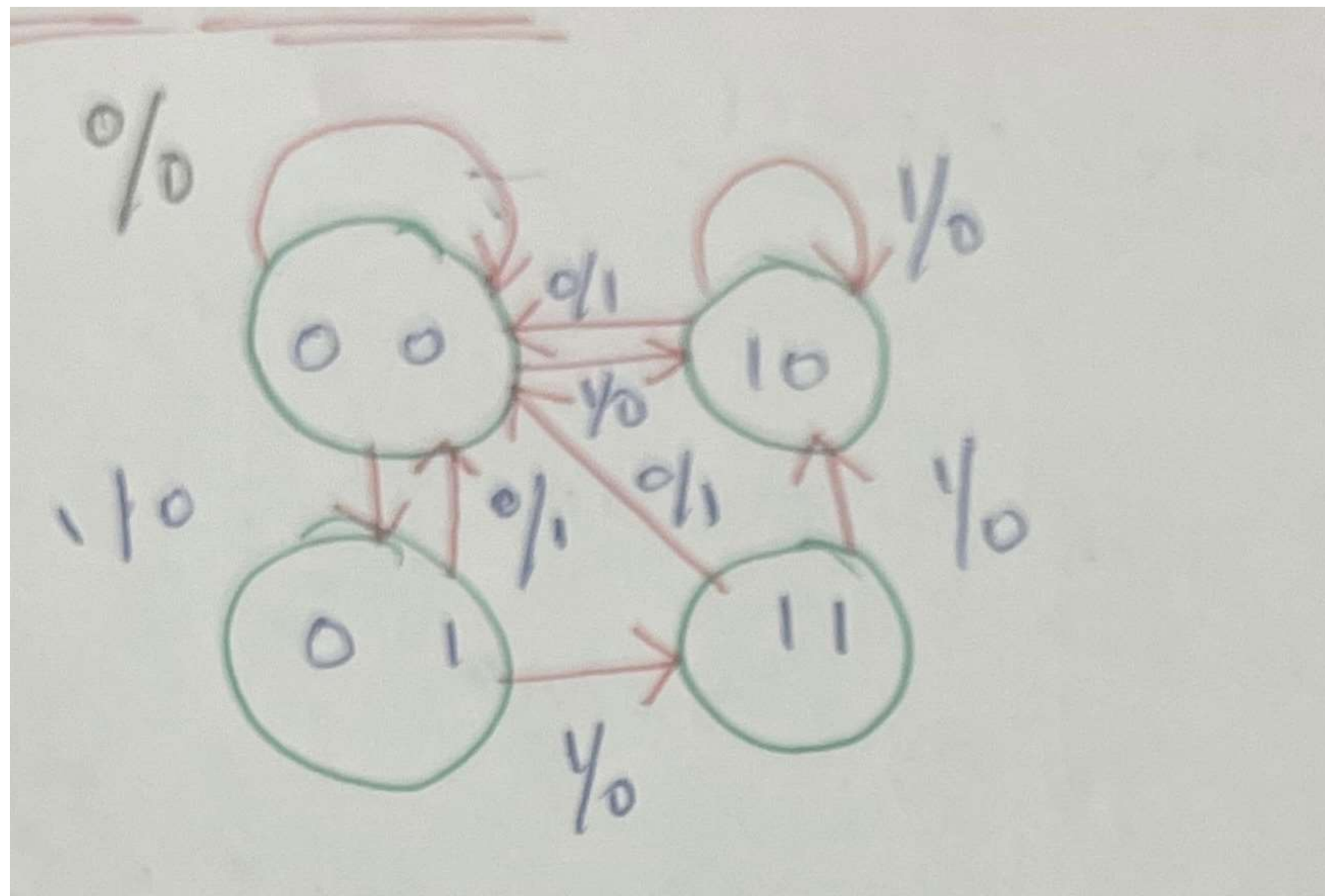
$$Y = (A+B)\bar{x}$$

STATE TABLE or TRANSITION TABLE

input x	Previous State		Next State		output Y
	A	B	A(t+1)	B(t+1)	
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	0	1
0	1	1	0	0	1
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	0



Analysis and design of clocked sequential circuits - Finite State Machines - Mealy Model





THANK YOU