Hard wired Control -

To execute instructions the processor must generate control signals needed in proper sequence.

2 Categories ⇒ 1) Hard wired control
2) Micro Programmed Control

Each ctrl signal will get completing its execution in one or many clock period.

The Required control signals are determined by the following information -

- ↳ Contents of control step counter.
- ↳ " " instruction register.
- ↳ " " Conditional code flags.
- ↳ External i/p signals, such as MFC & interrupt requests.

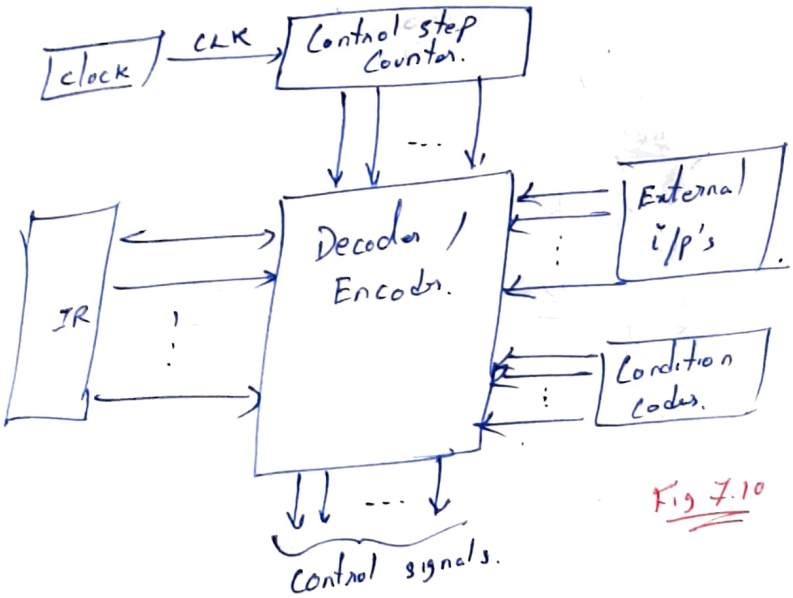
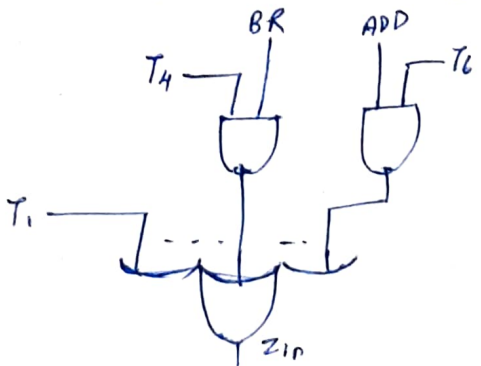


Fig 7.10 Control Unit Organization.

eg 1 generating ctrl signal for logic f/n $Z_{in} = T_1 + T_6 \cdot ADD + T_4 \cdot BR + \ldots$



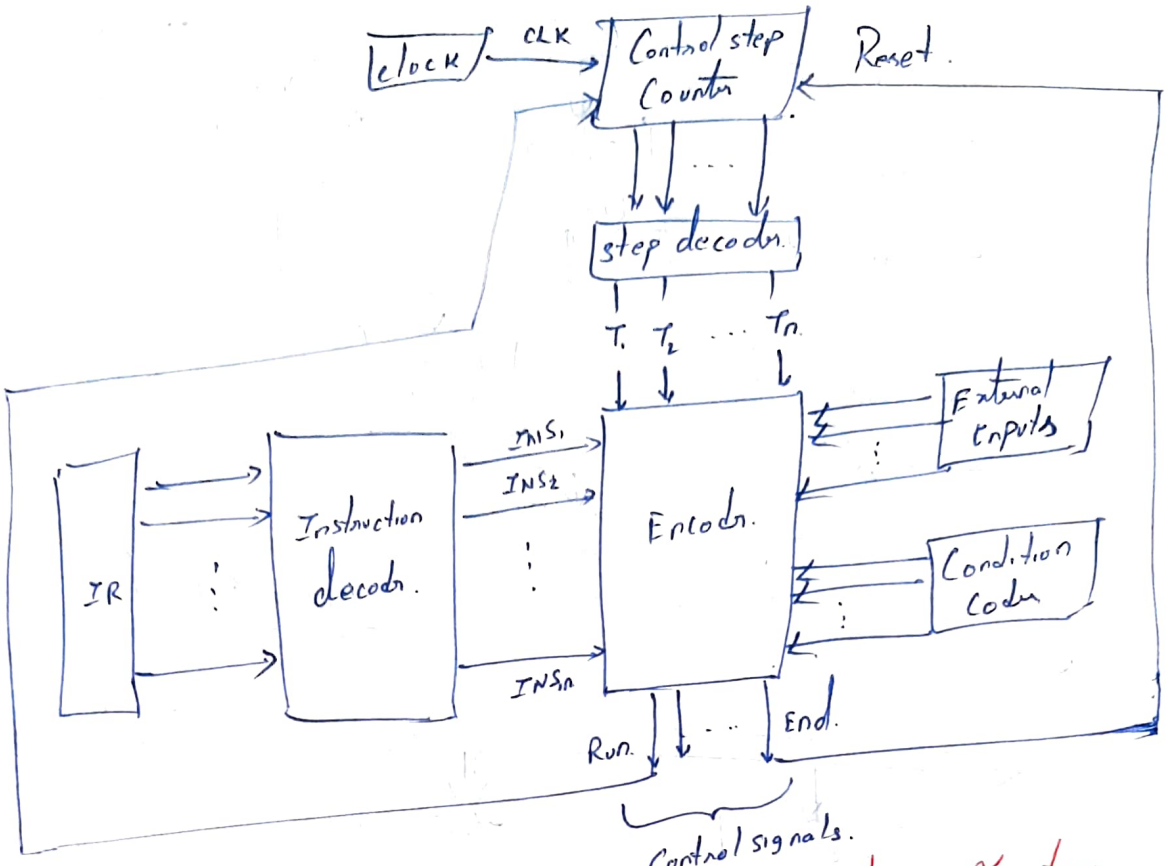


Fig 7.11 Operation of the decoding & encoding functions.

eg2 $End = T_7 \cdot ADD + T_5 \cdot BR + (T_5 \cdot N + T_4 \cdot \bar{N}) \cdot BRN + \ldots$

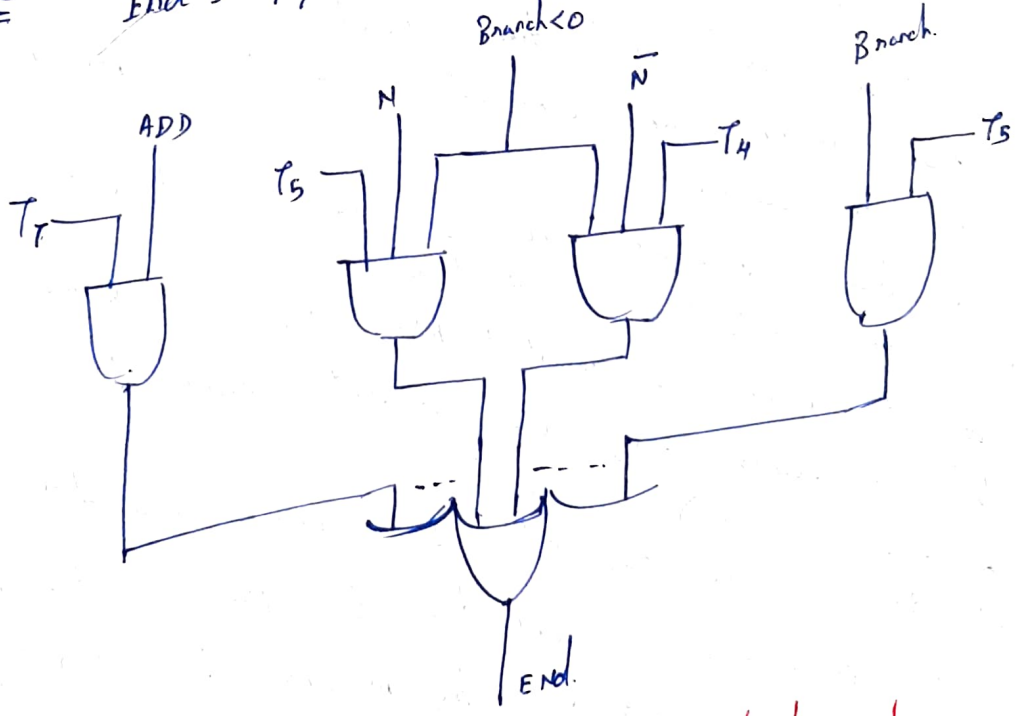


Fig 7.13 Generation of End control signal.

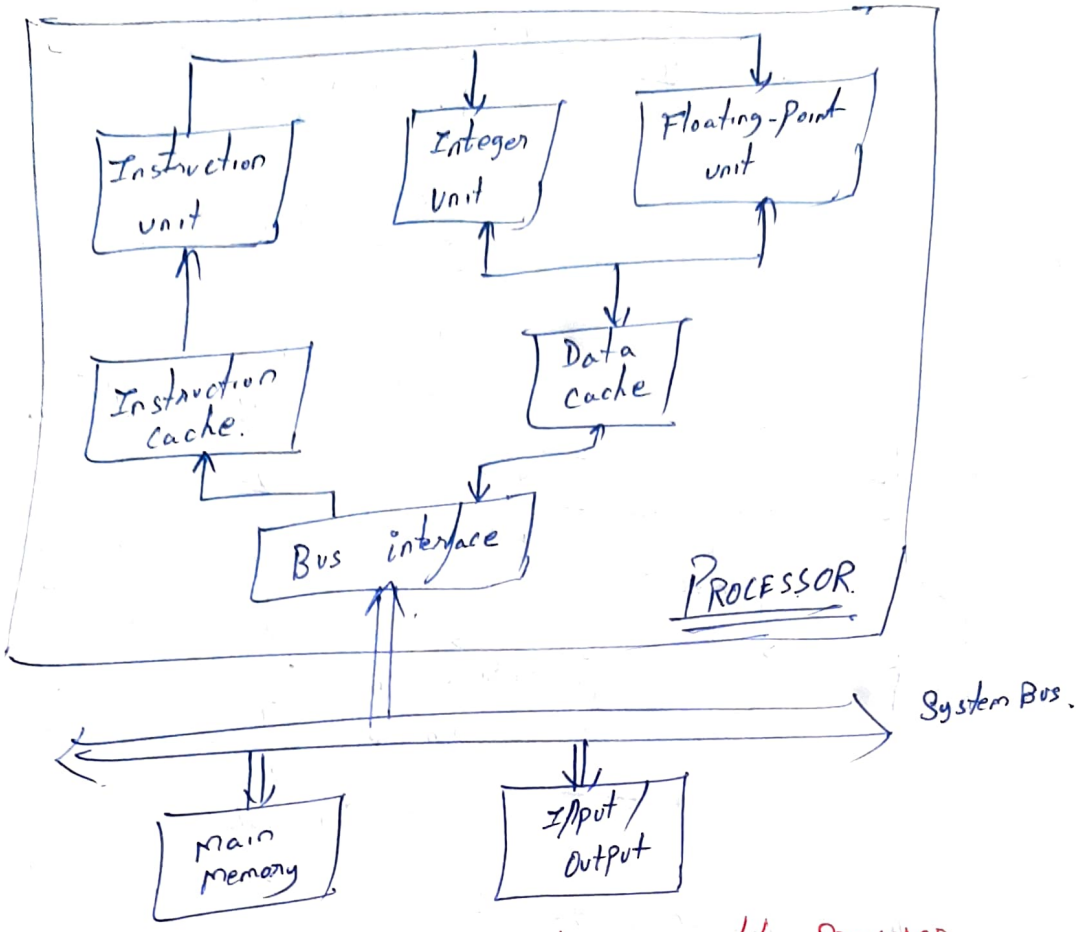


Fig 7.14 Block Diagram of a complete processor.

This structure has an instruction unit that fetches instructions from an instruction cache or from main memory, when the desired instructions are not already in the cache.

It has Depointe Processing units to deal with integer data and floating point data.

A Data cache is inserted b/w these units & main memory.

* the processors may use separate cache for instruction & Data. (or)
* A single cache can store both instruction & data.

The processor is connected to the system bus. & rest of the computer by means of a Bus Interface.