SNS COLLEGE OF TECHNOLOGY

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

23ECB201–DIGITAL SYSTEMS DESIGN

II YEAR/ III SEMESTER

UNIT 5–PROGRAMMABLE LOGIC DEVICES AND LOGIC FAMILIES

TOPIC - Implementation Of Combinational Logic Using

PROM,PLA,PAL

Implementation of combinational Logic Circuit using PAL

• Let us see the implementation of a combinational circuit using PAL with the help of examples.

Examples for Understanding

Ex. 9.4.1 Implement the following Boolean functions using PAL.

w (A, B, C,D) = $\sum m$ (0, 2, 6, 7, 8, 9, 12, 13),
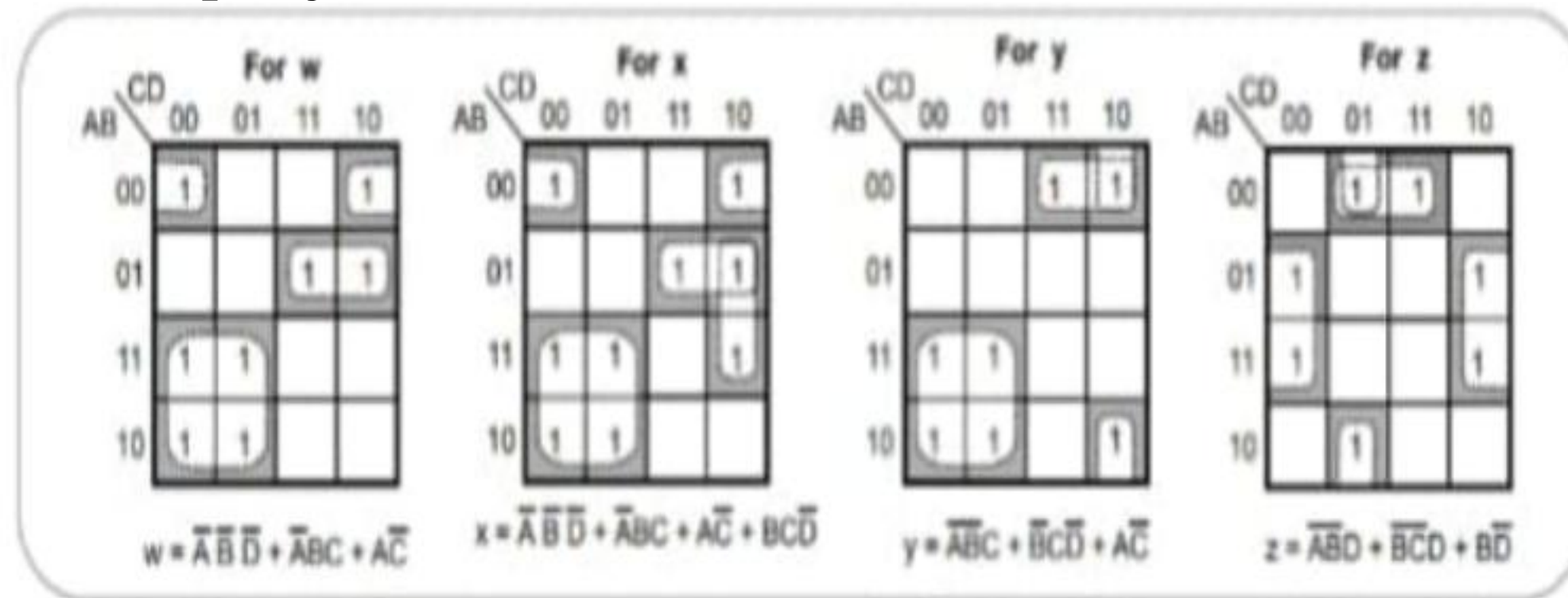
x (A,B,C,D) = $\sum m$ (0, 2, 6, 7, 8, 9, 12, 13, 14)

y (A,B,C,D) = $\sum m$ (2, 3, 8, 9, 10, 12,13), z (A,B,C,D) = $\sum m$ (1, 3, 4, 6, 9, 12, 14)

Step 1: Simplify the four functions

$$X = W + BCD'$$

Note that function x has four product terms. Three of them are equal to w. Therefore we can write

Step 2 : Implementation

In the last section we have seen the PLA program table. The program table for PAL is similar to PLA program table. Table 9.4.1 shows PAL program table with product terms, AND inputs and outputs.

Product term	AND Inputs					Outputs
	A	B	C	D	w	
1	0	0	–	0	–	$w = \overline{A}\,\overline{B}\,\overline{D} + \overline{A}\,BC + A\,\overline{C}$
2	0	1	1	–	–	
3	1	–	0	–	–	
4	–	–	–	–	1	$x = w + BC\overline{D}$
5	–	1	1	0	–	
6	–	–	–	–	–	
7	0	0	1	–	–	$y = \overline{A}\,\overline{B}\,C + \overline{B}\,C\,\overline{D} + A\,\overline{C}$
8	–	0	1	0	–	
9	1	–	0	–	–	
10	0	0	–	1	–	$z = \overline{A}\,\overline{B}\,D + \overline{B}\,\overline{C}\,D + B\,\overline{D}$
11	–	0	0	1	–	
12	–	1	–	0	–	

Table 9.4.1 PAL program table

Implementation of combinational Logic Circuit Using PAL

Fig. 9.4.3 Logic diagram

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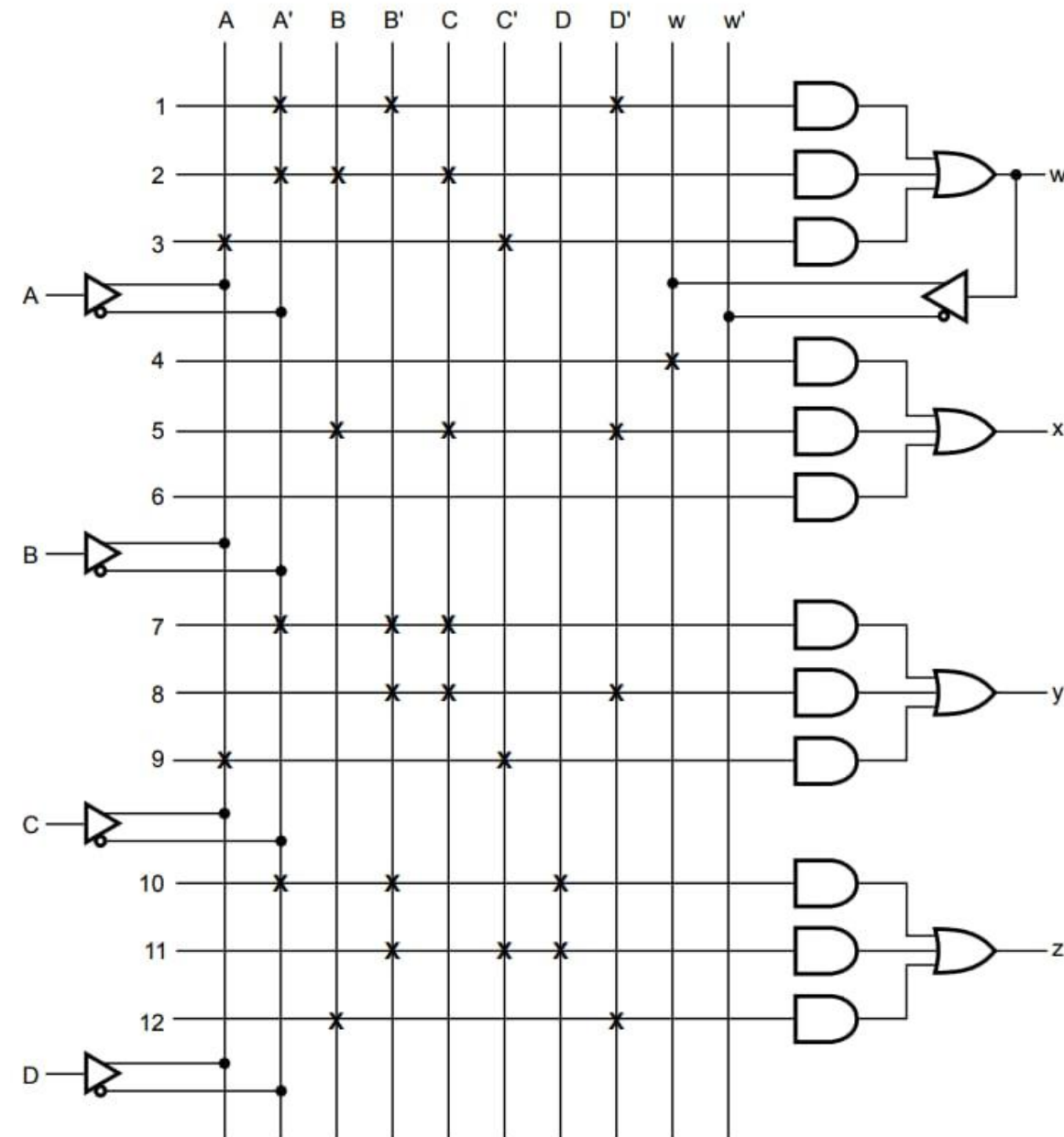
Implementation of combinational Logic Circuit using PAL

Design BCD to Excess-3 converter using PAL.

Step 1 : Derive the truth table of BCD to Excess-3 converter

Decimal	BCD code				Excess-3 code			
	B_3	B_2	B_1	B_0	E_3	E_2	E_1	E_0
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

Table 9.4.2 Truth table for BCD to Excess-3 code converter

Simplify the Boolean functions for Excess-3 code outputs.
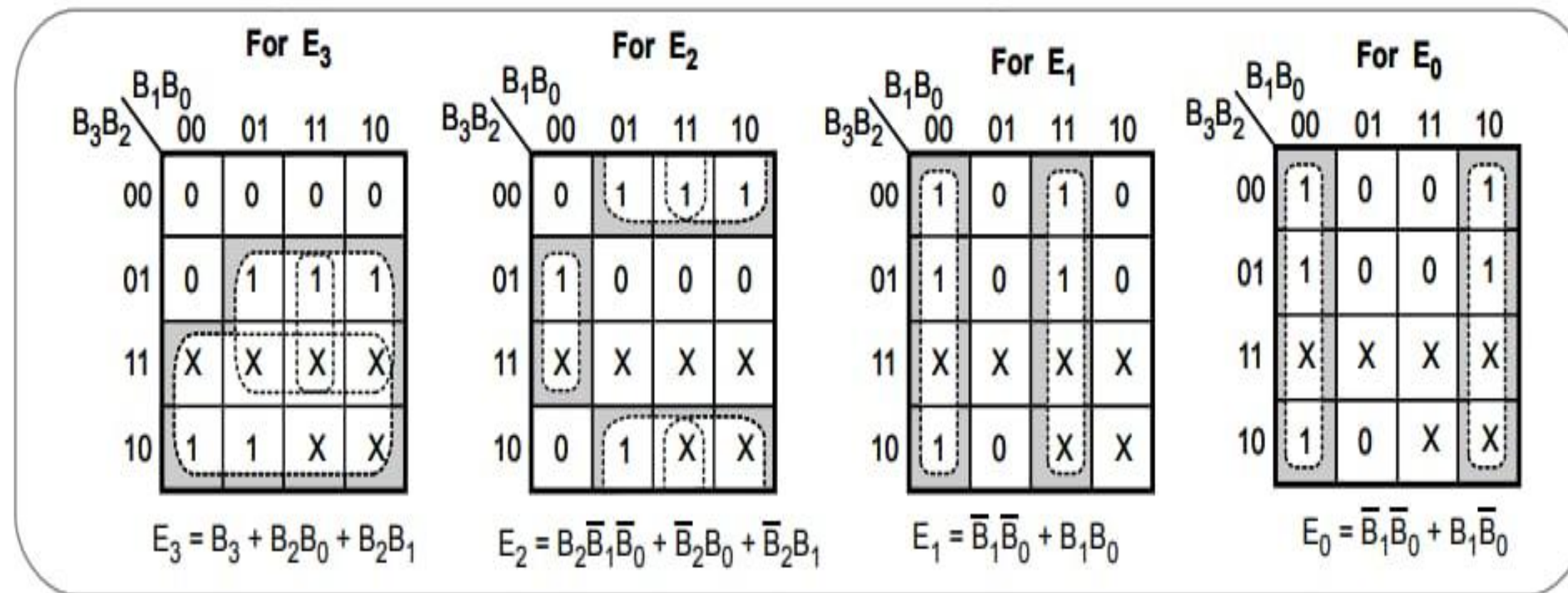
Fig. 9.4.4 K-map simplification

Step 3 : Implementation

Product terms		Inputs				Outputs			
		B_3	B_2	B_1	B_0	E_3	E_2	E_1	E_0
B_3	1	1	–	–	–	1	–	–	–
$B_2 B_0$	2	–	1	–	1	1	–	–	–
$B_2 B_1$	3	–	1	1	–	1	–	–	–
$B_2 \overline{B}_1 \overline{B}_0$	4	–	1	0	0	–	1	–	–
$\overline{B}_2 B_0$	5	–	0	–	1	–	1	–	–
$\overline{B}_2 B_1$	6	–	0	1	–	–	1	–	–
$\overline{B}_1 \overline{B}_0$	7	–	–	0	0	–	–	1	1
$B_1 B_0$	8	–	–	1	1	–	–	1	–
$B_1 \overline{B}_0$	9	–	–	1	0	–	–	–	1
						T	T	T	T	T/C

Table 9.4.3 PAL program table

Implementation of combinational Logic Circuit using PAL

Fig. 9.4.5 Logic diagram

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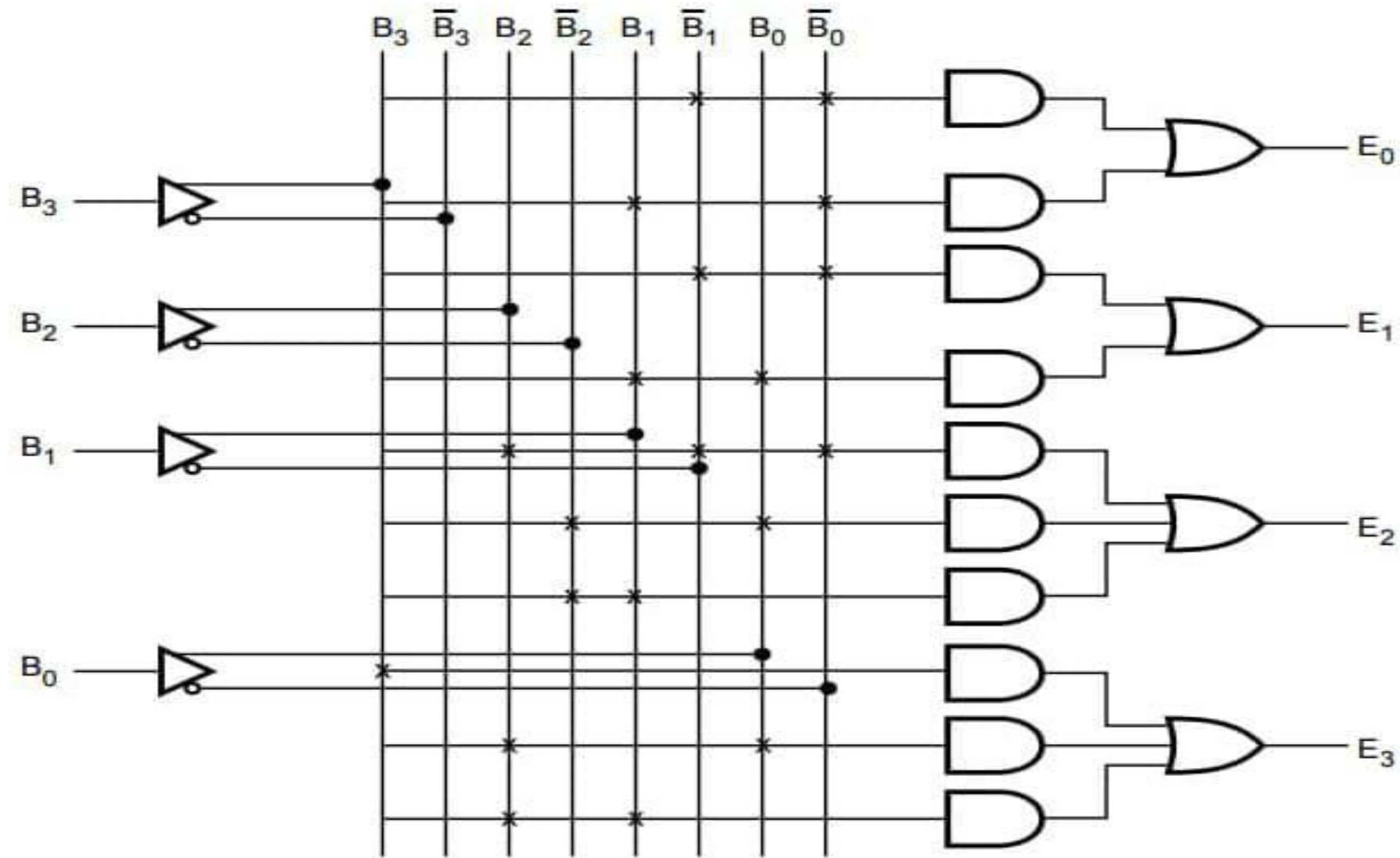
Implementation of combinational Logic Circuit using PLA

Step 1: Truth Table

Table 1: BCD to Excess-3 Code Conversion

INPUT (BCD CODE)				OUTPUT (EXCESS-3 CODE)			
B_3	B_2	B_1	B_0	E_3	E_2	E_1	E_0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	X	X	X	X

Implementation of combinational Logic Circuit using PLA

1	0	1	1	X	X	X	X
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

Step 2: K-Map

Implementation of combinational Logic Circuit using PLA

E3= B3 + B2B0 + B2B1

 | | |

 (1) (2) (3)

E2= B2B1 + B2B0 + B2B1B0

 | | |

 (4) (5) (6)

E1= B1B0 + B1B0

 | |

 (7) (8)

E0 =B0

 |

 (9)

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Implementation of combinational Logic Circuit using PLA

Step 3: Prepare the PLA program tabl$_e$

Table 2: PLA programming table

Product term No.	Product term	I/P				O/P			
		B3	B2	B1	B0	E3	E2	E1	E0
1	B3	1	–	–	–	1	–	–	–
2	B2B0	–	1	–	1	1	–	–	–
3	B2B1	–	1	1	–	1	–	–	–
4	$\overline{B2}$B1	–	0	1	–	–	1	–	–
5	$\overline{B2}$B0	–	0	–	1	–	1	–	–
6	B2$\overline{B1}$ $\overline{B0}$	–	1	0	0	–	1	–	–

Implementation of combinational Logic Circuit using PLA

7	$\overline{B1B0}$	-	-	0	0	-	-	1	-
8	B1B0	-	-	1	1	-	-	1	-
9	$\overline{B0}$	-	-	-	0	-	-	-	1

Step 4: Implementation of the PLA circuit

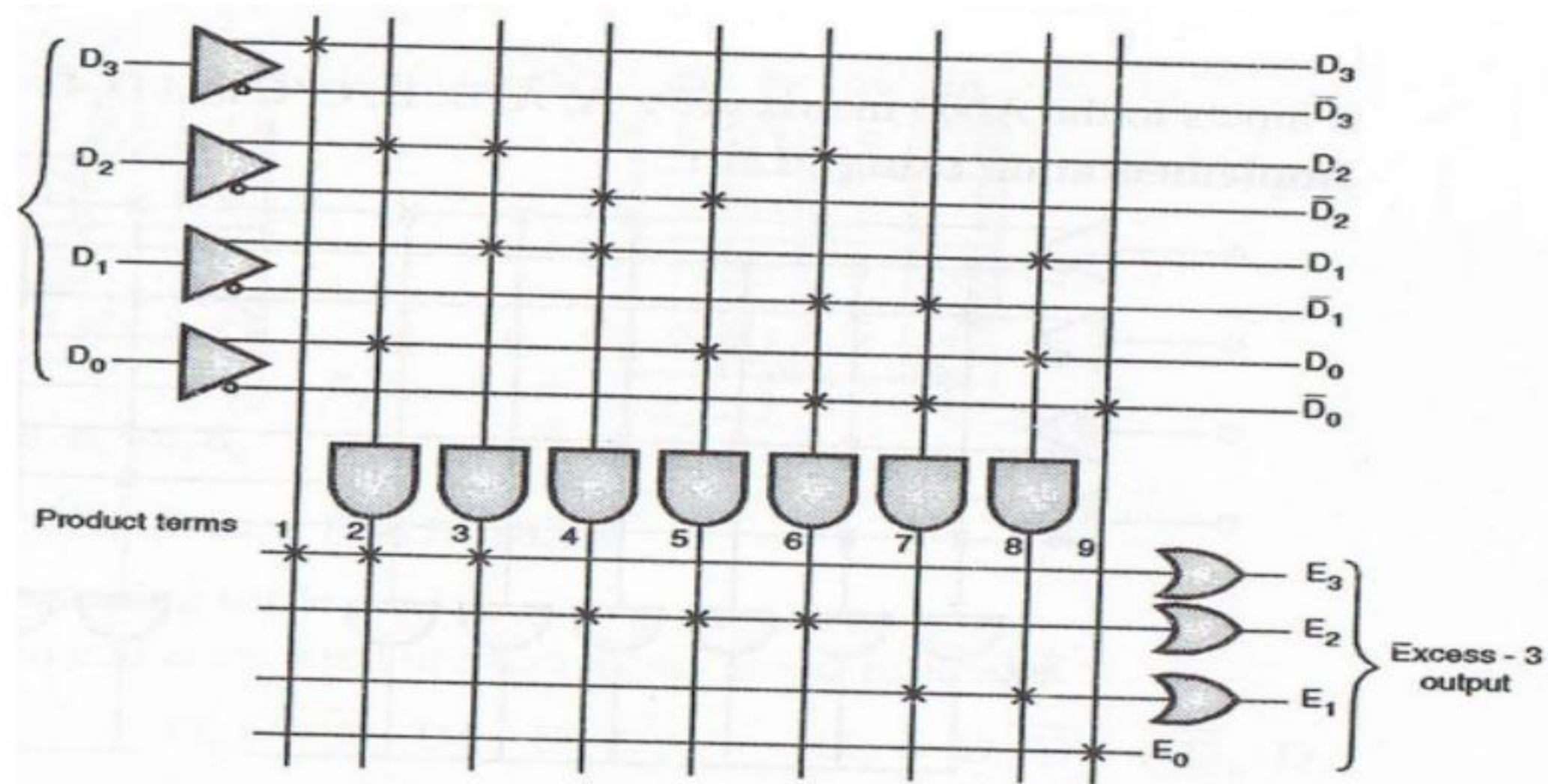The logic circuit for BCD to Excess-3 converter using a PLA device

Fig 3: PLA logic circuit for BCD to Excess-3 Convertor

Implementation of combinational Logic Circuit using PROM

Design a combinational circuit using PROM to convert gray code into binary code.

STEP 1: Truth Table for Grey to

GRAY INPUT			BINARY OUTPUT (Y)		
G2	G1	G0	B2	B1	B0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	1	0	1	0
0	1	0	0	1	1
1	1	0	1	0	0
1	1	1	1	0	1
1	0	1	1	1	0
1	0	0	1	1	1

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STEP2 : Simplification by using K map

$$B_2 = G_2 \text{------(1)}$$

$$B_1 = G_2\,\overline{G}_1 + \overline{G}_2\,G_1 \text{------(2)}$$

$$B_0 = \overline{G}_2\overline{G}_1 G_0 + \overline{G}_2 G_1\overline{G}_0 \text{-----(3)}$$

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Syed Hasan Saeed, Integral University, Lucknow

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STEP 3:
No. of inputs 3
No. of address lines (locations) = 2 ^ 3 = 8
Each location can store 4 bit words
No. of outputs = 4 (B_3 B_2 B_1 B_0)

ROM Programming Table: (with the help of Eq. 1, 2 and 3)

ROM Programming Table: (with the help of Eq. 1, 2 and 3)

Location No.	Inputs			Outputs			
	G_2	G_1	G_0	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	1
2	0	1	0	0	0	1	1
3	0	1	1	0	0	1	0
4	1	0	0	0	1	1	1
5	1	0	1	0	1	1	0
6	1	1	0	0	1	0	0
7	1	1	1	0	1	0	1

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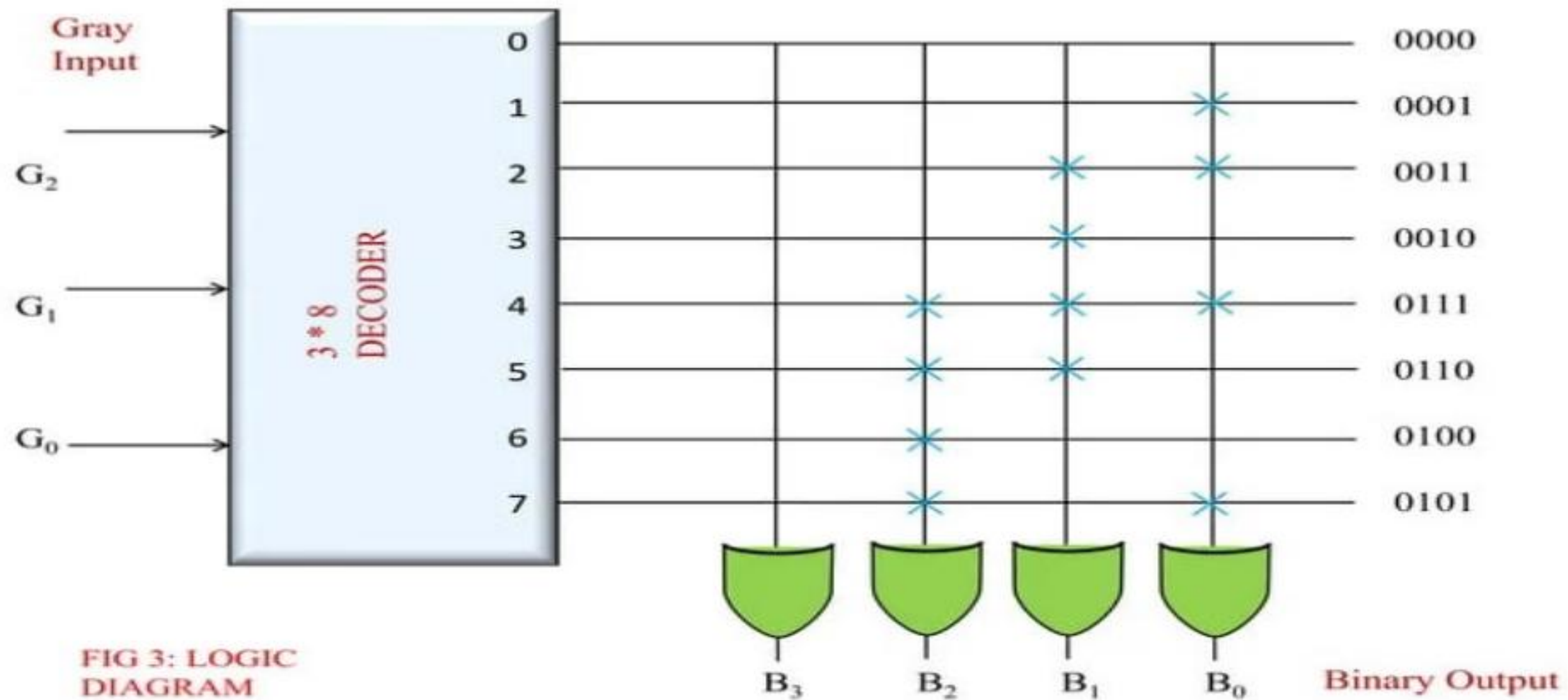
Implementation of combinational Logic Circuit using PROM

FIG 3: LOGIC DIAGRAM

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THANK YOU