

# **SNS COLLEGE OF TECHNOLOGY**

**Coimbatore-35 An Autonomous Institution** 

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# **DEPARTMENT OF ELECTRONICS & COMMUNICATION** ENGINEERING

# **19ECT312 – EMBEDDED SYSTEM DESIGN**

Embedded Memory /19ECT312/Embedded systems Design / Mrs.E.Ramya/AP/ECE/SNSCT

III YEAR/ VI SEMESTER

**UNIT 1 – INTRODUCTION TO EMBEDDED SYSTEMS** 

TOPIC 7 – EMBEDDED MEMORY





- 1. Basic Memory types
- 2. Basic Memory Organization
- 3. Definitions of RAM, ROM and Cache Memory
- 5. Difference between Static and Dynamic RAM
- 6. Various Memory Control Signals
- 7. Memory Specifications
- 8. Basics of Memory Interfacing





### **Processor Memory**, **Primary Memory**, **Memory Interfacing**

Most of the modern computer system has been designed on the basis of an architecture called Von-Neumann Architecture1



The Von Neumann Architecture

The Memory stores the instructions as well as data. No one can distinguish an instruction and data. The CPU has to be directed to the address of the instruction codes.

The memory is connected to the CPU through the following lines

- 1.Address
- 2.Data
- 3.Control









### In a memory read operation

- the CPU loads the address onto the address bus. ullet
- Most cases these lines are fed to a decoder which selects the proper memory location. •
- The CPU then sends a read control signal. ullet
- The data is stored in that location is transferred to the processor via the data lines. •





In the memory write operation after the address is loaded the CPU sends the write control signal followed by the data to the requested memory location.

The memory can be classified in various ways i.e. based on the location, power consumption, way of data storage etc

### The memory at the basic level can be classified as

- 1. Processor Memory (Register Array)
- 2. Internal on-chip Memory
- 3. Primary Memory
- 4. Cache Memory
- 5. Secondary Memory







### **Processor Memory (Register Array)**

- •Most processors have some registers associated with the arithmetic logic units.
- •They store the operands and the result of an instruction.
- •The data transfer rates are much faster without needing any additional clock cycles.
- •The number of registers varies from processor to processor.
- •The more is the number the faster is the instruction execution.
- •But the complexity of the architecture puts a limit on the amount of the processor memory.







### Internal on-chip Memory

- •In some processors there may be a block of memory location.
- •They are treated as the same way as the external memory. However it is very fast. **Primary Memory**
- •This is the one which sits just out side the CPU.
- •It can also stay in the same chip as of CPU.
- •These memories can be static or dynamic.

### Cache Memory

- •This is situated in between the processor and the primary memory.
- •This serves as a buffer to the immediate instructions or data which the processor anticipates. There can be more than one levels of cache memory.





- •These are generally treated as Input/Output devices.
- •They are much cheaper mass storage and slower devices connected through some input/output interface circuits.
- •They are generally magnetic or optical memories such as Hard Disk and CDROM devices.
- •The memory can also be divided into Volatile and Non-volatile memory.
- Volatile Memory
- •The contents are erased when the power is switched off.
- •Semiconductor Random Access Memories fall into this category. Non-volatile Memory

The contents are intact even of the power is switched off. Magnetic Memories (Hard Disks), Optical Disks (CDROMs), Read Only Memories (ROM) fall under this category.





### **Internal view**



The example of a ROM with decoder and data storage

### **Implementation of Combinatorial Functions**

•Any combinational circuit of *n* functions of same *k* variables can be done with  $2^k \ge n$  ROM.

- •The inputs of the combinatorial circuit are the address of the ROM locations.
- •The output is the word stored at that location.







RAM: "Random-access" memory

- •Typically volatile memory
  - bits are not held without power supply
- •Read and written to easily by embedded system during execution
- •Internal structure more complex than ROM
  - a word consists of several memory cells, each storing 1 bit
  - -each input and output data line connects to each cell in its column
  - -rd/wr connected to every cell
  - when row is enabled by decoder, each cell has logic that stores input data
    - bit when rd/wr indicates write or outputs stored bit when rd/wr indicates read











The RAM decoder and access







Basic types of RAM

•SRAM: Static RAM

- Memory cell uses flip-flop to store bit

- Requires 6 transistors

-Holds data as long as power supplied

•DRAM: Dynamic RAM

- Memory cell uses MOS transistor and capacitor to store bit

- More compact than SRAM

- "Refresh" required due to capacitor leak

Embedded Memory /19ECT312/Embedded systems Design / Mrs.E.Ramya/AP/ECE/SNSCT WORD S CEIIS refreshed when read









# Data





**Ram variations** 

- DRAM with built-in memory refresh controller
- Popular low-cost high-density alternative to SRAM
- •NVRAM: Nonvolatile RAM
  - -Holds data after external power removed
  - Battery-backed RAM
    - •SRAM with own permanently connected battery
    - •writes as fast as reads

### •no limit on number of writes unlike nonvolatile ROM-based memory

Embedded Memory /19ECT312/Embedded systems Design / Mrs.E.Ramya/AP/ECE/SNSCT - CDAM with EEDDOM on floch stores complete DAM contents on EEDDOM on





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Example: HM6264 & 27C256 RAM/ROM devices

- •Low-cost low-capacity memory devices
- •Commonly used in 8-bit microcontroller-based embedded systems
- •First two numeric digits indicate device type
  - **–** RAM: 62
  - **—** ROM: 27
- •Subsequent digits indicate capacity in kilobits





### Assessment

1.List the types of memory

2.Compare ROM and RAM

3. What is EPROM?







### **SUMMARY & THANK YOU**

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