SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)

Coimbatore-35

DEPARTMENT OF BIOMEDICAL ENGINEERING

19BMB303 & Fundamentals of Microprocessors and Microcontrollers

UNIT II – 8259 INTERFACING

III Year/ VI Sem

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ASP / BME / SNSCT

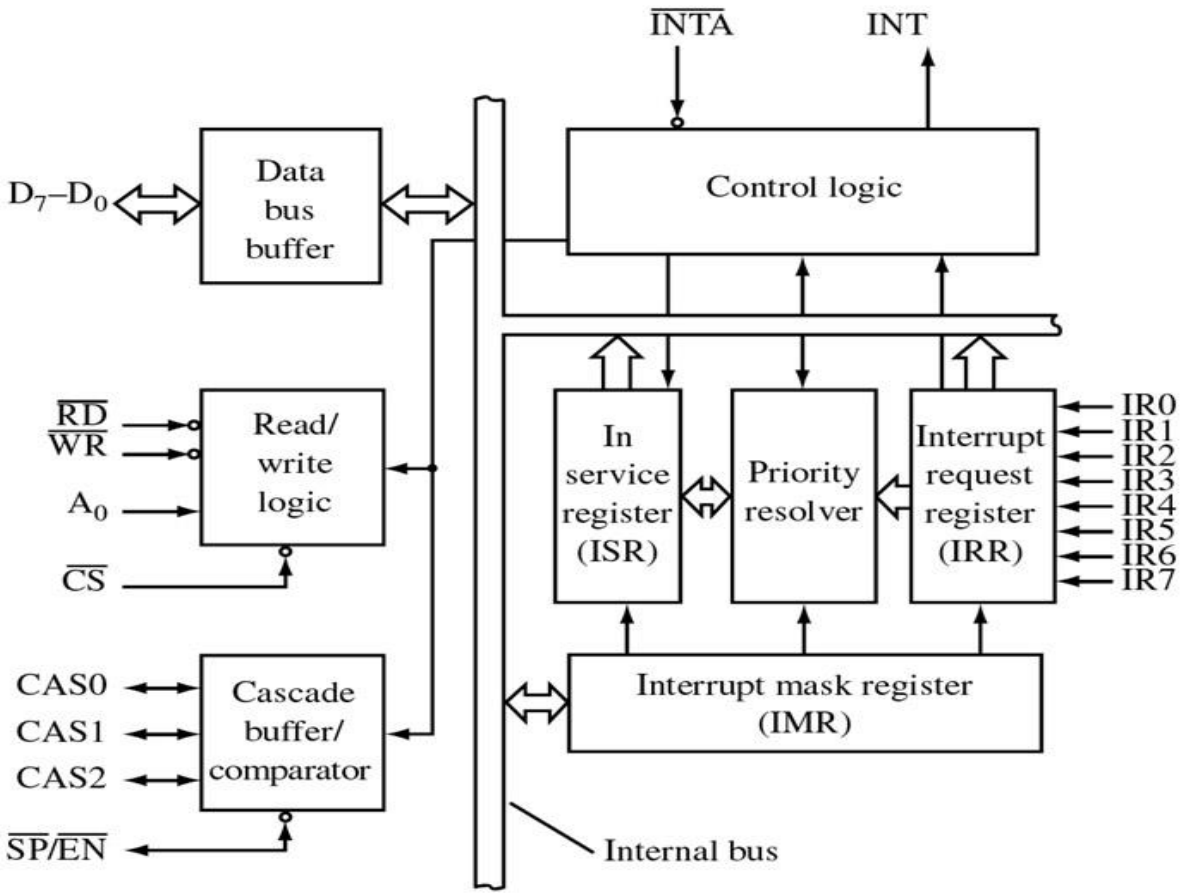
8259

- 8259 is Programmable Interrupt Controller (PIC)
- It is a tool for managing the interrupt requests.
- 8259 is a very flexible peripheral controller chip:
  - PIC can deal with up to 64 interrupt inputs
  - interrupts can be masked
  - various priority schemes can also programmed.
- originally (in PC XT) it is available as a separate IC
- Later the functionality of *(two PICs)* is in the motherboards chipset.
- In some of the modern processors, the functionality of the *PIC* is built in.

Pin description

- 8-bit bi-directional data bus, one address line is needed,

  PIC has two control registers to be programmed, you can think of them as two output ports or two memory location.
- The direction of data flow is controlled by RD and WR.
- CS is as usual connected to the output of the address decoder.
- Interrupt requests are output on INT which is connected to the INTR of the processor. Int. acknowledgment is received by INTA.
- IR0-IR7 allow 8 separate interrupt requests to be inputted to the PIC.
- sp/en=1 for master , sp/en=0 for slave.
- CAS0-3 inputs/outputs are used when more than one PIC to cascaded.


INTA
INT
Data bus buffer
D7–D0
Control logic
RD
WR
A0
CS
Read/ write logic
In service register (ISR)
Priority resolver
Interrupt request register (IRR)
IR0
IR1
IR2
IR3
IR4
IR5
IR6
IR7
CAS0
CAS1
CAS2
Cascade buffer/ comparator
SP/EN
Interrupt mask register (IMR)
Internal bus

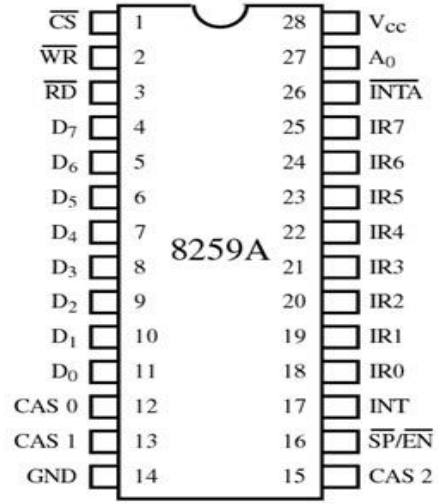

CS 1
WR 2
RD 3
D7 4
D6 5
D5 6
D4 7
D3 8
D2 9
D1 10
D0 11
CAS 0 12
CAS 1 13
GND 14
8259A
28 Vcc
27 A0
26 INTA
25 IR7
24 IR6
23 IR5
22 IR4
21 IR3
20 IR2
19 IR1
18 IR0
17 INT
16 SP/EN
15 CAS 2

FIGURE 9-5 Interfacing the PIC to the 386 and 486 processors. Two I/O ports are required.

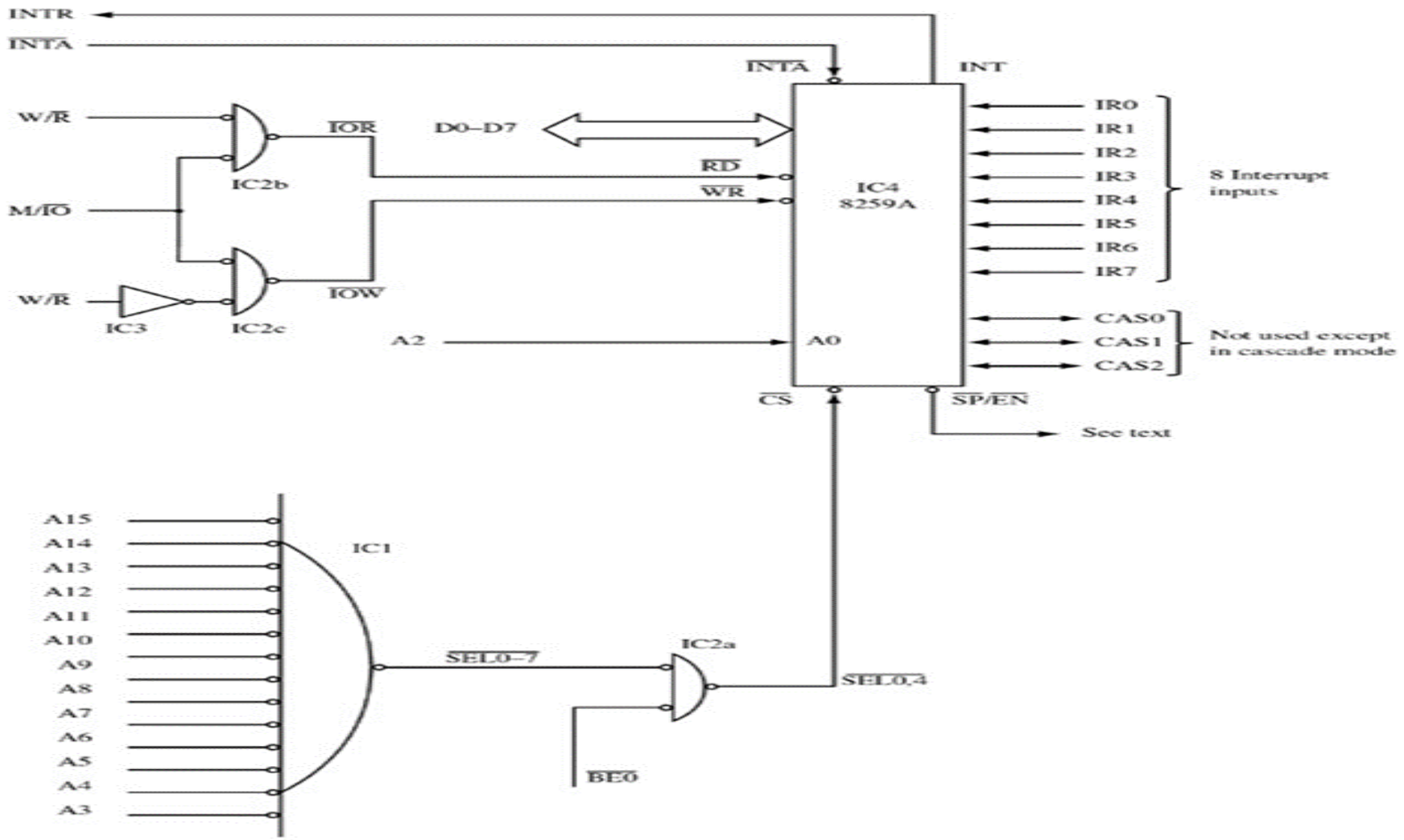
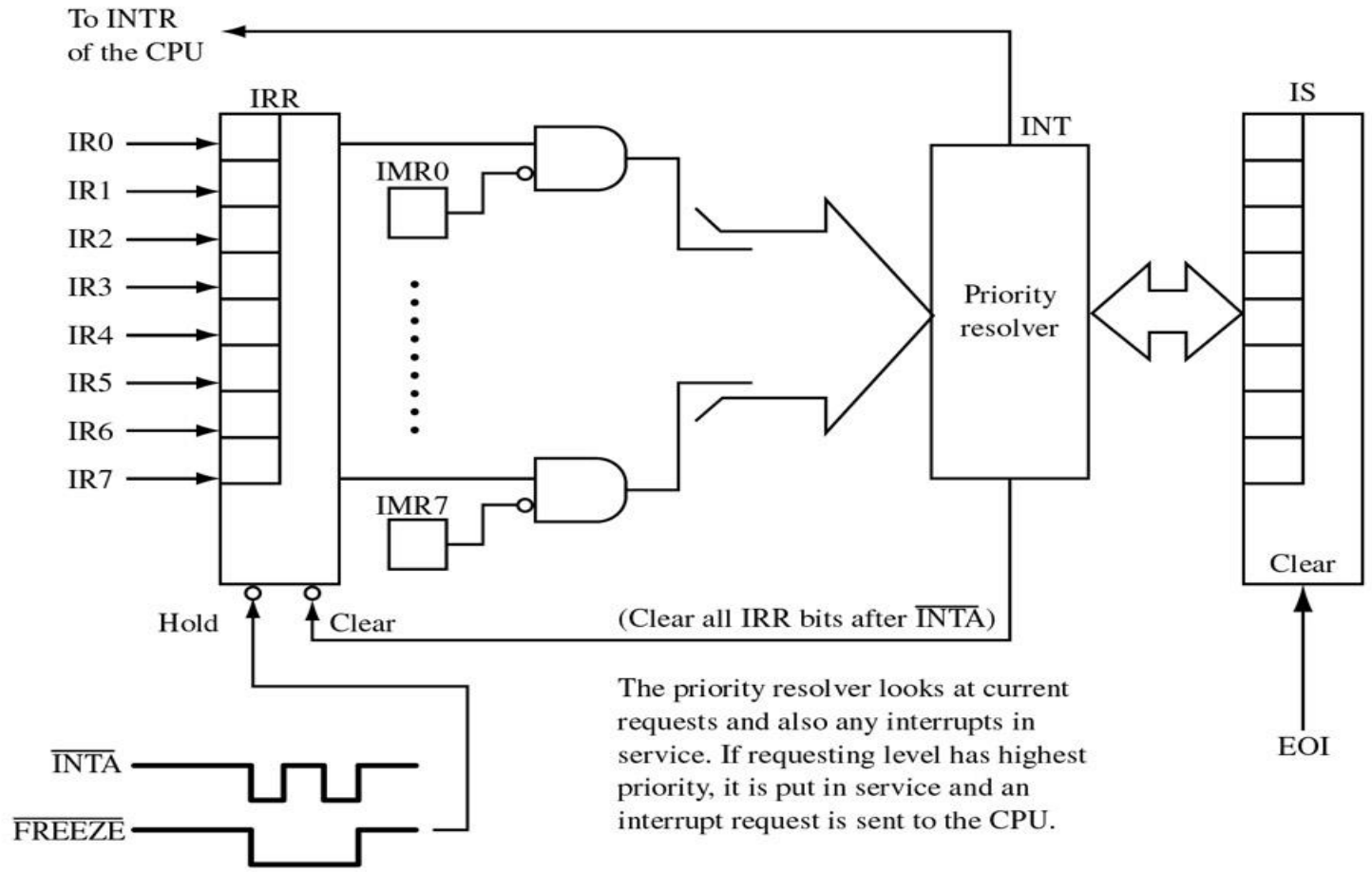
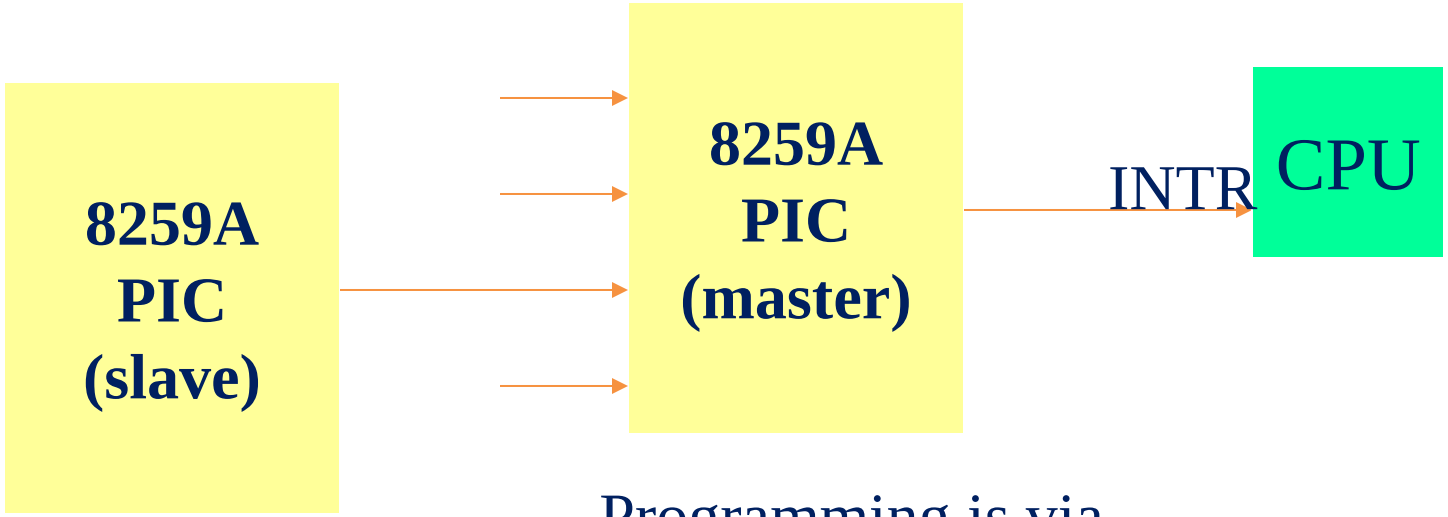


FIGURE 9-7 All interrupt requests must pass through the PIC's interrupt request register (IRR) and interrupt mask register (IMR). If put in service, the appropriate bit of the in-service (IS) register is set.





Programming is via
I/O-ports 0xA0-0xA1

Programming is via
I/O-ports 0x20-0x21

Initialization Command Word 1