Memory Management -Segmentation with Paging
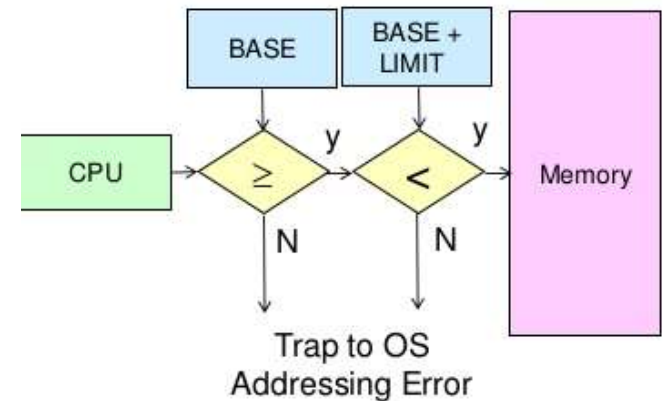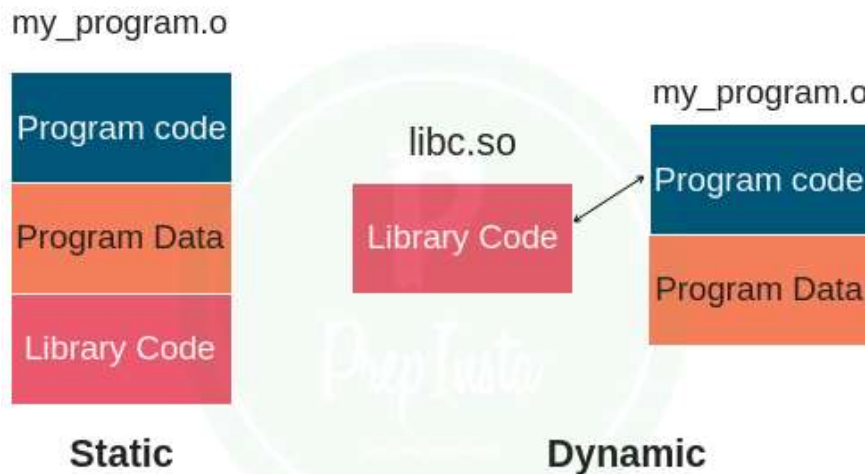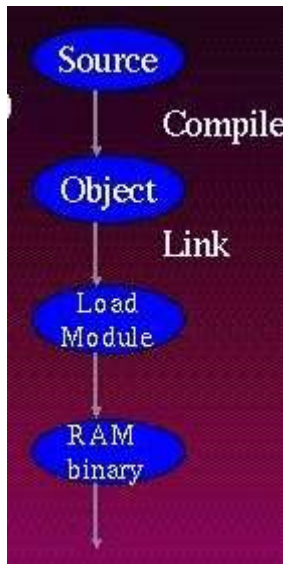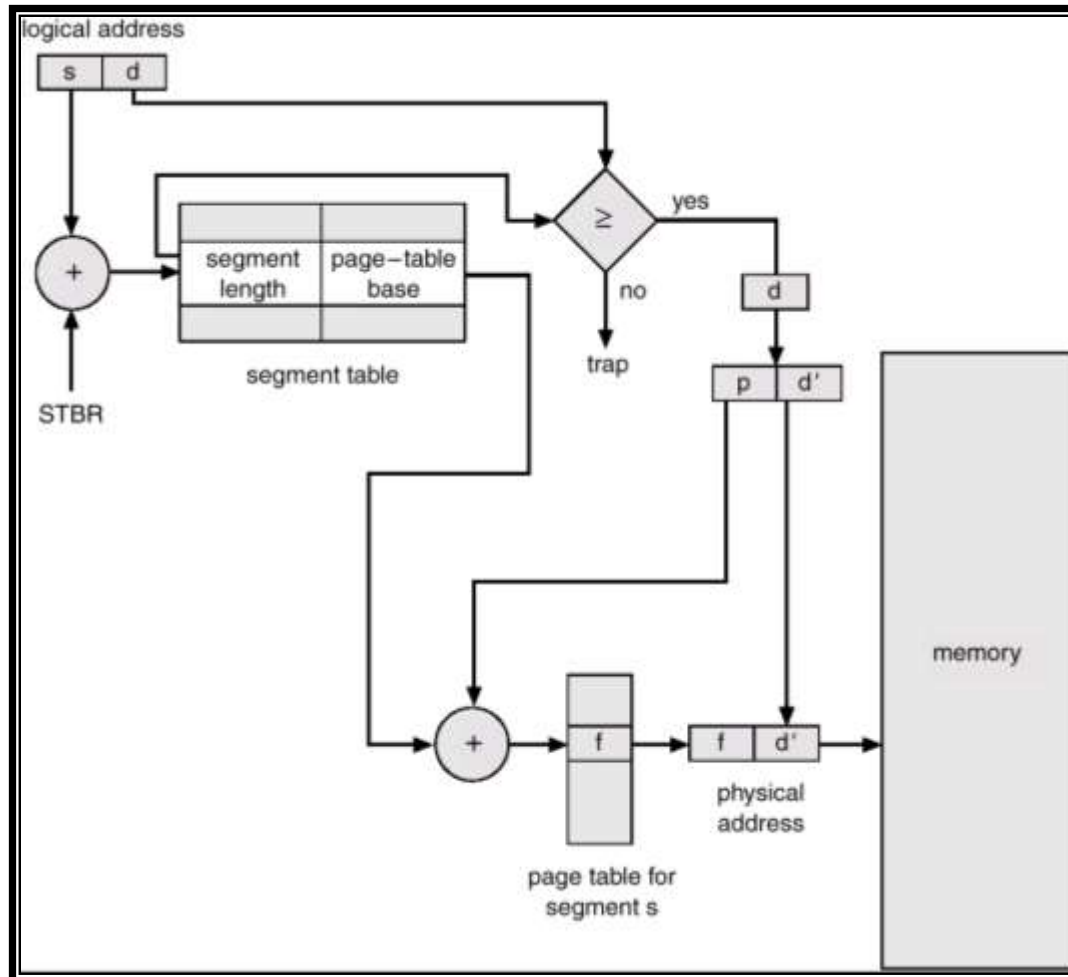
Segmentation with Paging – MULTICS

- The MULTICS system solved problems of external fragmentation and lengthy search times by paging the segments.

- Solution differs from pure segmentation in that the segment-table entry contains not the base address of the segment, but rather the base address of a *page table* for this segment.
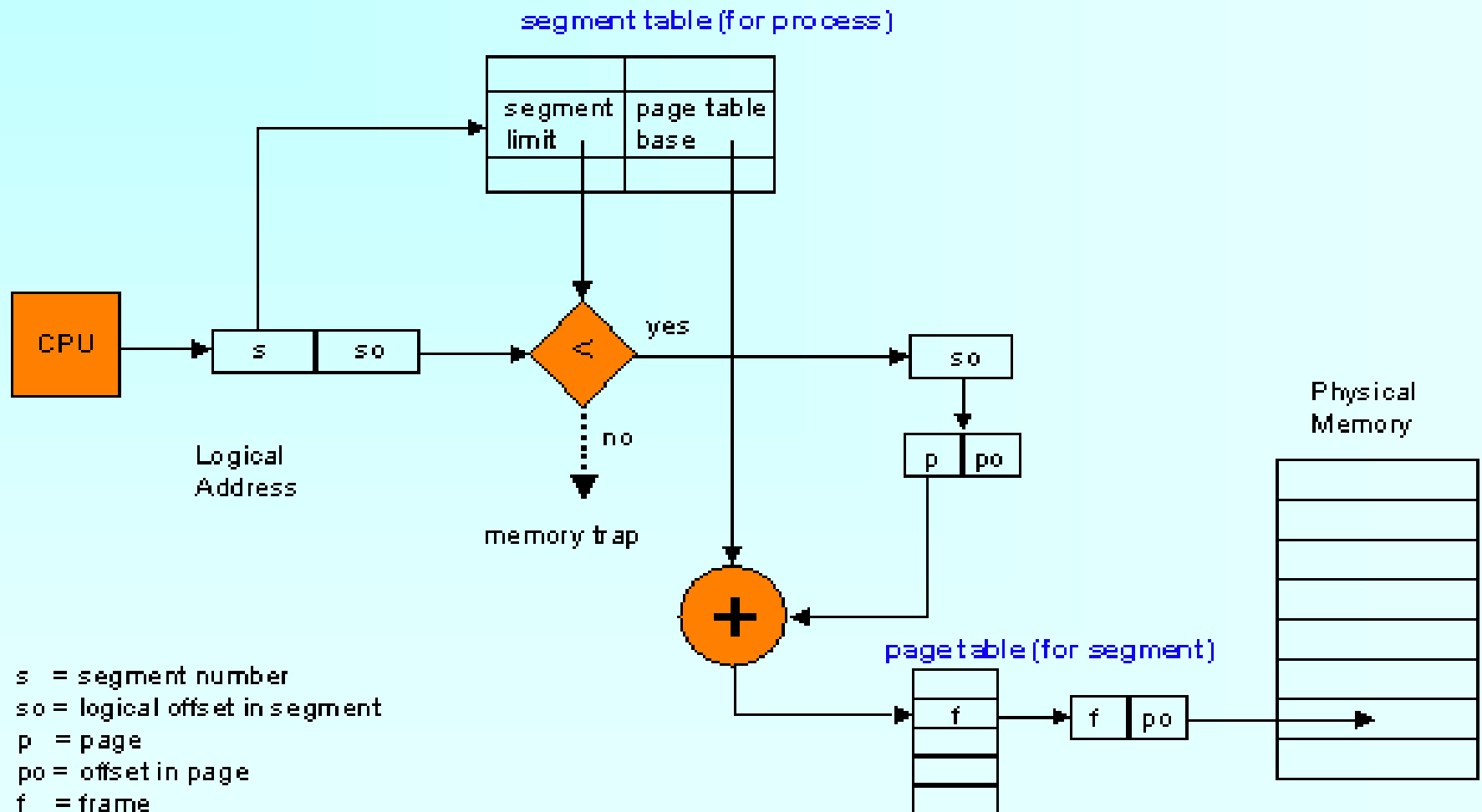
MULTICS Address Translation Scheme

Segmentation with Paging – Intel 386

- As shown in the following diagram, the Intel 386 uses segmentation with paging for memory management with a two-level paging scheme.

Architecture for Segmentation with Paging

segment table (for process)

segment limit	page table base

CPU

s	so

Logical Address

< yes → so

no

memory trap

p	po

+

Physical Memory

page table (for segment)

f

f	po

s = segment number
so = logical offset in segment
p = page
po = offset in page
f = frame

4/3/2025

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Summarization

23CST202- OS-Segmentation with paging-
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