SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A++' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECT312 – EMBEDDED SYSTEM DESIGN

III YEAR/ VI SEMESTER

UNIT 1 – **INTRODUCTION TO EMBEDDED SYSTEMS**

TOPIC 1–5 RISC Architecture

RISC ARCHITECTURE

A Reduced Instruction Set Computer is a type of microprocessor architecture that utilizes a small, highly-optimized set of instructions rather than the highly-specialized set of instructions typically found in other architectures.

Who defined RISC architecture?

IBM -1970.

RISC (Reduced Instruction Set Computer) is a microprocessor that is designed to perform a smaller number of instructions so that it can operate faster.

RISC VS CISC

What is the difference between RISC and CISC architecture?

RISC

- **decoding of instructions is simple.**
- RISC doesn't require external memory for calculations.
- RISC has multiple register sets are present.

CISC

- **decoding of instructions is complex**
- CISC requires external memory for calculations,
- only a single register set while

RISC ARCHITECTURE

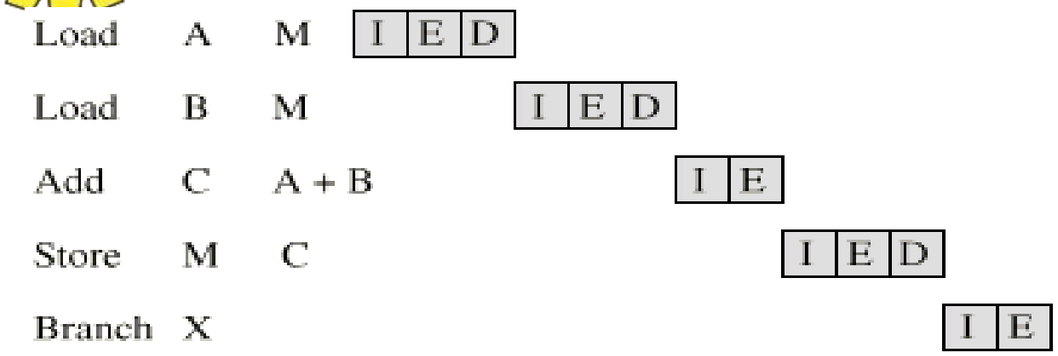
RISC Characteristics

- One instruction per cycle
- Register to register operations
- Few, simple addressing modes
- Few, simple instruction formats
- Hardwired design (no microcode)
- Fixed instruction format
- More compile time/effort
- Instruction comes undersize of one word.
- Simpler instruction, hence simple instruction decoding.
- Instruction takes a single clock cycle to get executed.
- More general-purpose registers. Simple Addressing Modes

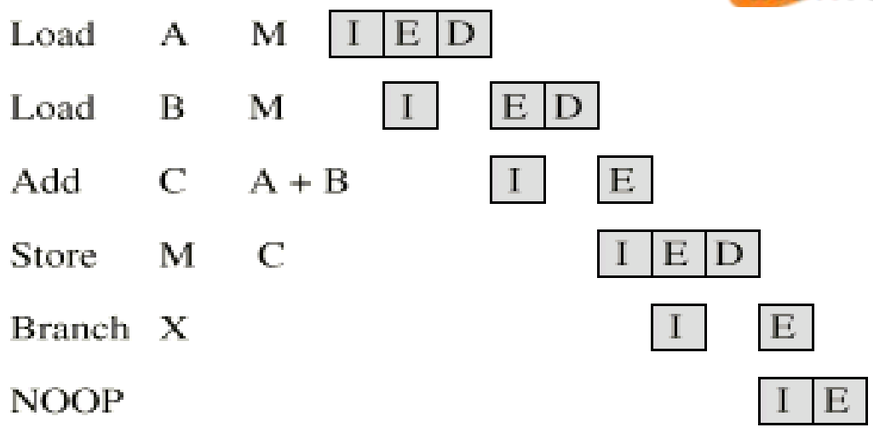
RISC Pipelining

- Most instructions are register to register
- Two phases of execution
  - I: Instruction fetch
  - E: Execute
    - ALU operation with register input and output
- For load and store
  - I: Instruction fetch
  - E: Execute
    - Calculate memory address
  - D: Memory
    - Register to memory or memory to register operation

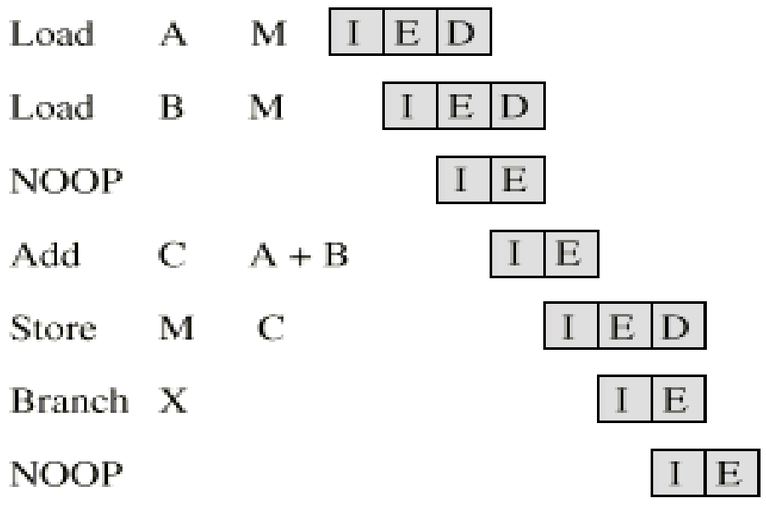
RISC ARCHITECTURE



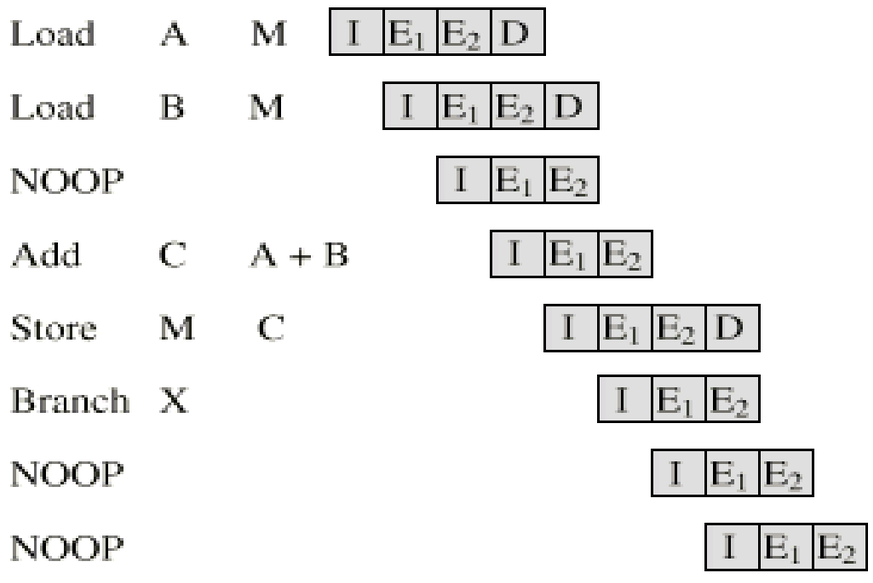
(a) Sequential execution



(b) Two-way pipelined timing



(c) Three-way pipelined timing



(d) Four-way pipelined timing

Effects of Pipelining

Optimization of Pipelining

- Delayed branch
  - Does not take effect until after execution of following instruction
  - This following instruction is the delay slot

Normal and Delayed Branch

Address	Normal	Delayed	Optimized
100	LOAD X,A	LOAD X,A	LOAD X,A
101	ADD 1,A	ADD 1,A	JUMP 105
102	JUMP 105	JUMP 105	ADD 1,A
103	ADD A,B	NOOP	ADD A,B
104	SUB C,B	ADD A,B	SUB C,B
105	STORE A,Z	SUB C,B	STORE A,Z
106		STORE A,Z0	

RISC ARCHITECTURE

Instruction Set Architecture

- A very important abstraction
  - interface between hardware and low-level software
  - standardizes instructions, machine language bit patterns, etc.
  - advantage: *different implementations of the same architecture*
  - disadvantage: *sometimes prevents using new innovations*

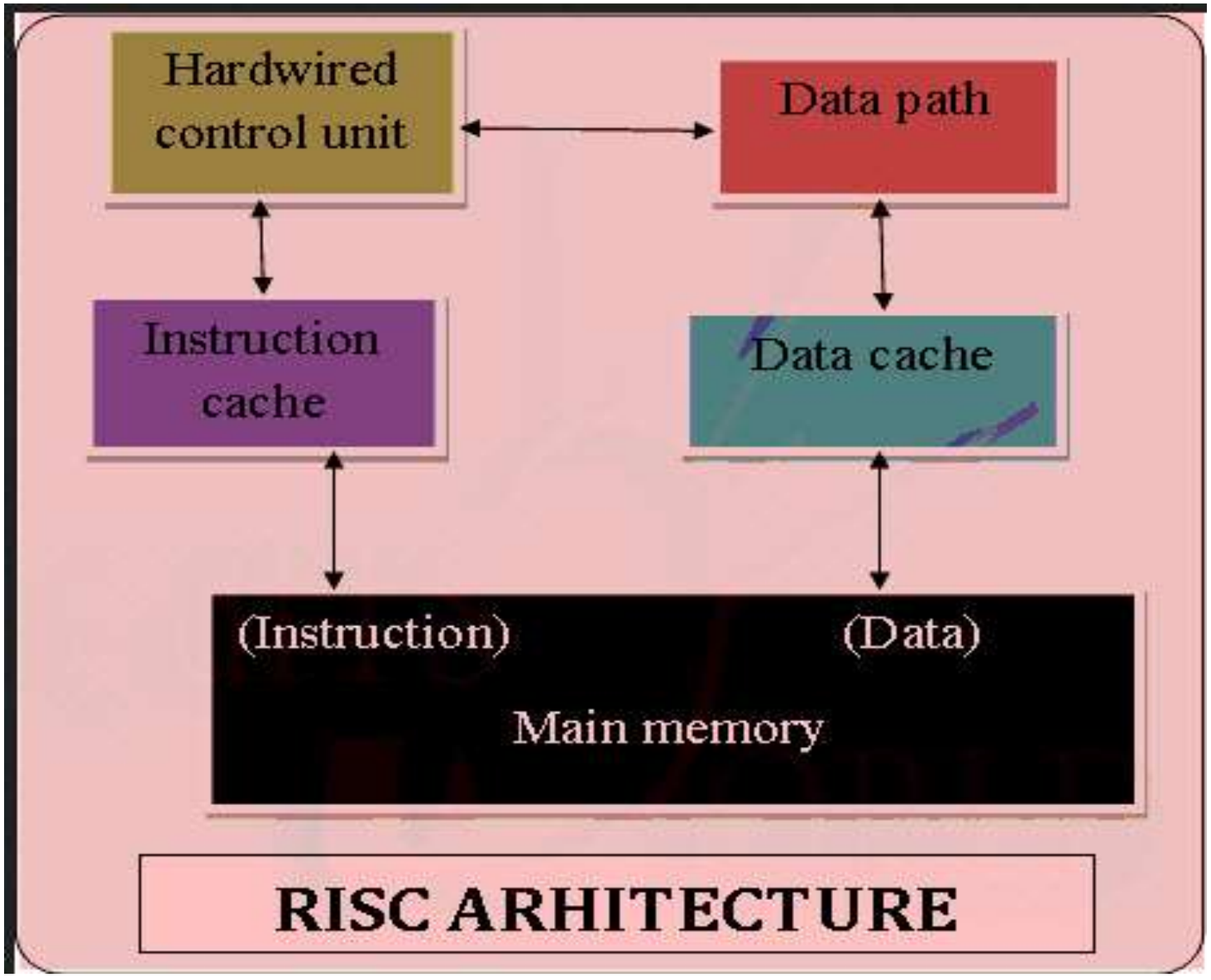
  True or False: Binary compatibility is extraordinarily important?

- Modern instruction set architectures:
  - IA-32, PowerPC, MIPS, SPARC, ARM, and others

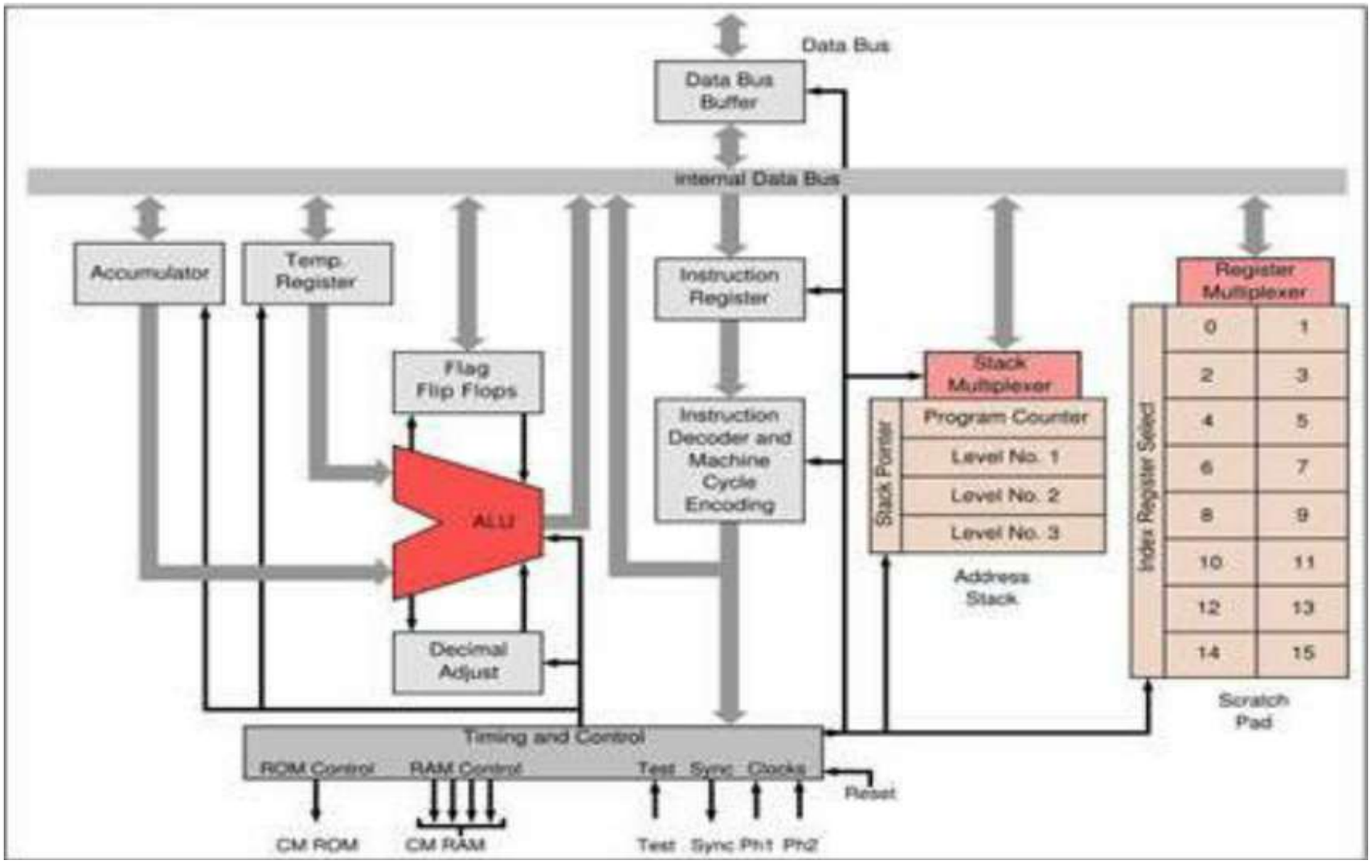
RISC ARCHITECTURE

ACTIVITY

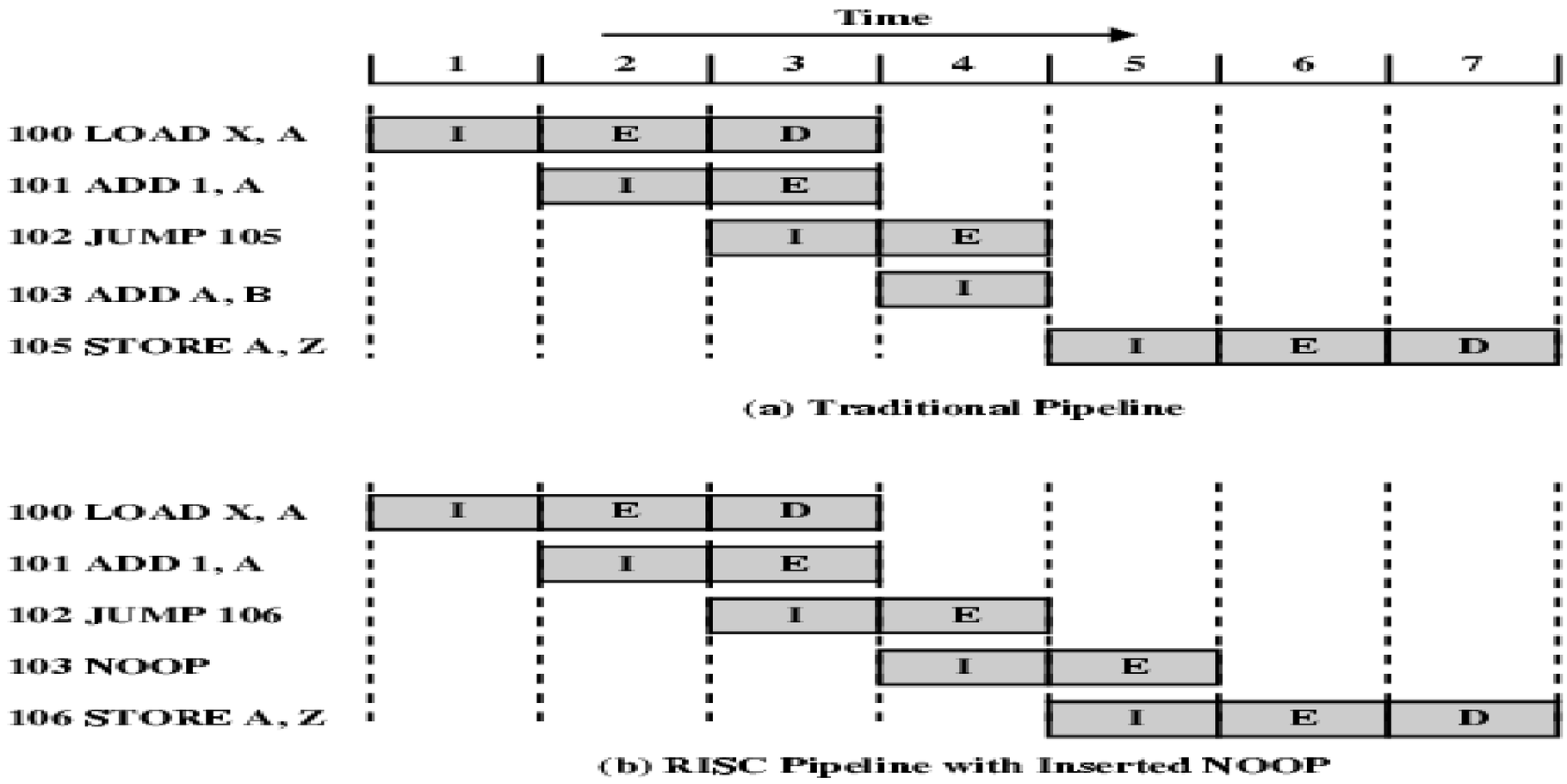
RISC ARCHITECTURE



64 bit -RISC ARCHITECTURE

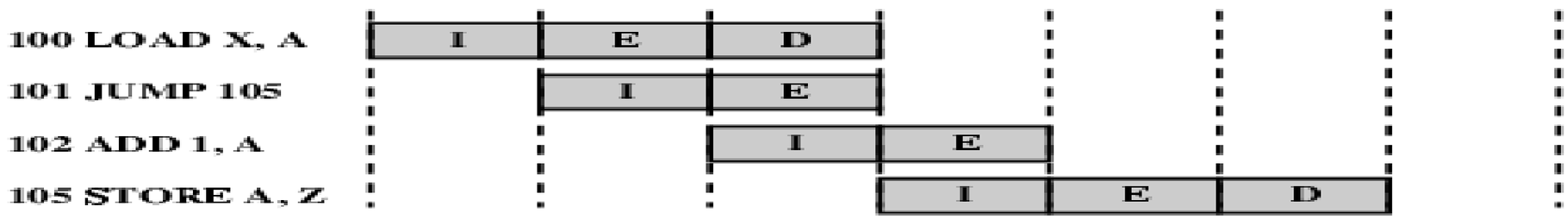


USE OF DELAYED BRANCH



(a) Traditional Pipeline

(b) RISC Pipeline with Inserted NOOP



(c) Reversed Instructions

RISC ARCHITECTURE

Controversy

- Quantitative
  - compare program sizes and execution speeds
- Qualitative
  - examine issues of high level language support and use of VLSI real estate
- Problems
  - No pair of RISC and CISC that are directly comparable
  - No definitive set of test programs
  - Difficult to separate hardware effects from complier effects
  - Most comparisons done on “toy” rather than production machines
  - Most commercial devices are a mixture

SUMMARY & THANK YOU