



SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution



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Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

23ECB202 – LINEAR INTEGRATED CIRCUITS

II YEAR/ III SEMESTER
1

UNIT 4 – ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTER

TOPIC 4.4 – Single Slope type & Dual Slope type





Single Slope Type - ADC

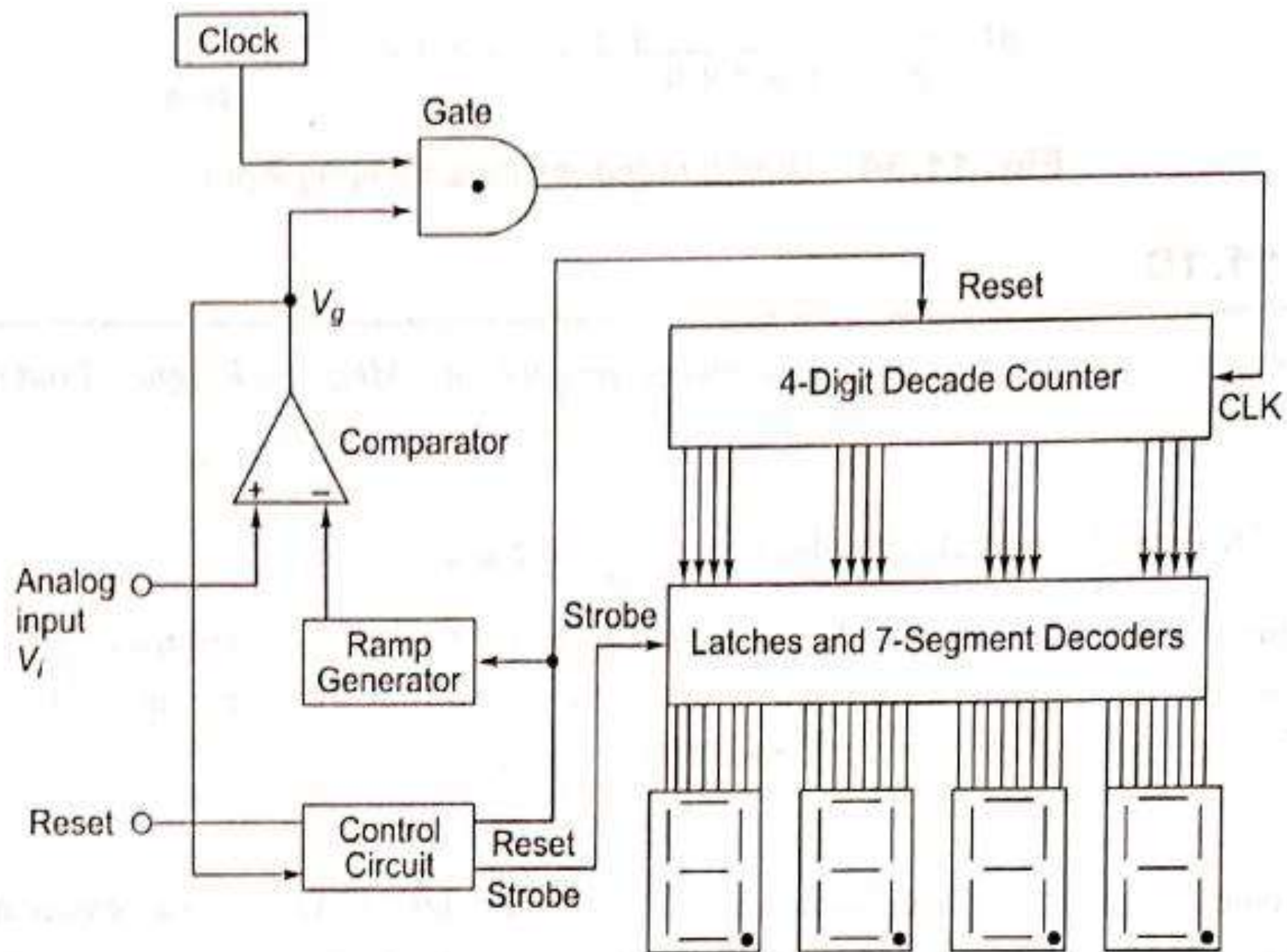


- A Single-Slope Integrating Type ADC is a type of analog-to-digital converter that converts an analog input signal into a digital output through the process of integration
- This ADC employs a ramp signal that is linearly increased or decreased, allowing it to measure the time taken for the ramp voltage to equal the input voltage
- The time duration is then quantified to represent the digital equivalent of the analog signal.





Single Slope Type - ADC





Single Slope Type - ADC



- These converter techniques are based on comparing the unknown analog i/p voltage with a reference voltage that begins at 0v & increases linearly with time
- The time required for the reference voltage to reach the value of unknown analog i/p voltage is proportional to the amplitude of unknown analog i/p voltage
- The time period can be measured using a digital counter. The main circuit of this converter is a ramp generator which on receiving a RESET from the control circuit increases linearly with time from 0v to a max volt V_m . Assume a +ive analog i/p voltage V_i is applied at the non-inverting i/p of the comparator
- When a RESET signal is applied to the control logic, the 4-digit decade counter resets to 0 & the ramp begins to increase. V_i is +ive the comparator o/p is in HIGH state.





Single Slope Type - ADC



- This allows the clk pulse to pass to the i/p of the 4-digit counter through the AND gate & the counter is incremented
- This process continues until the analog i/p voltage is greater than the ramp generator voltage
- When the ramp generator voltage is equal to the analog i/p voltage, the comparator o/p becomes negatively saturated or logic 0
- The clk is prevented from passing through the gate causing the counter operation
- Then the control circuit generates a STROBE signal, which latches the counter values in the 4-digit latch, which is displayed on 7-segment displays
- The displayed value is then equivalent to the amplitude of analog input voltage.





Dual Slope Type - ADC



- The analog part of the circuit consists of a high input impedance buffer A1, precision integrator A2 and a voltage comparator
- The converter first integrates the analog input signal V_a for a fixed duration of $2n$ clk periods
- Then it integrates an internal reference voltage V_R of opposite polarity until the integrator output is zero
- Before the START command arrives, the switch SW1 is connected to ground and SW2 is closed. Any offset voltage present in the A1, A2, comparator loop after integration appears across the capacitor CAZ till the threshold of the comparator is achieved
- The capacitor CAZ thus provides automatic compensation for the input-offset voltages of all the three amplifiers.





Dual Slope Type - ADC

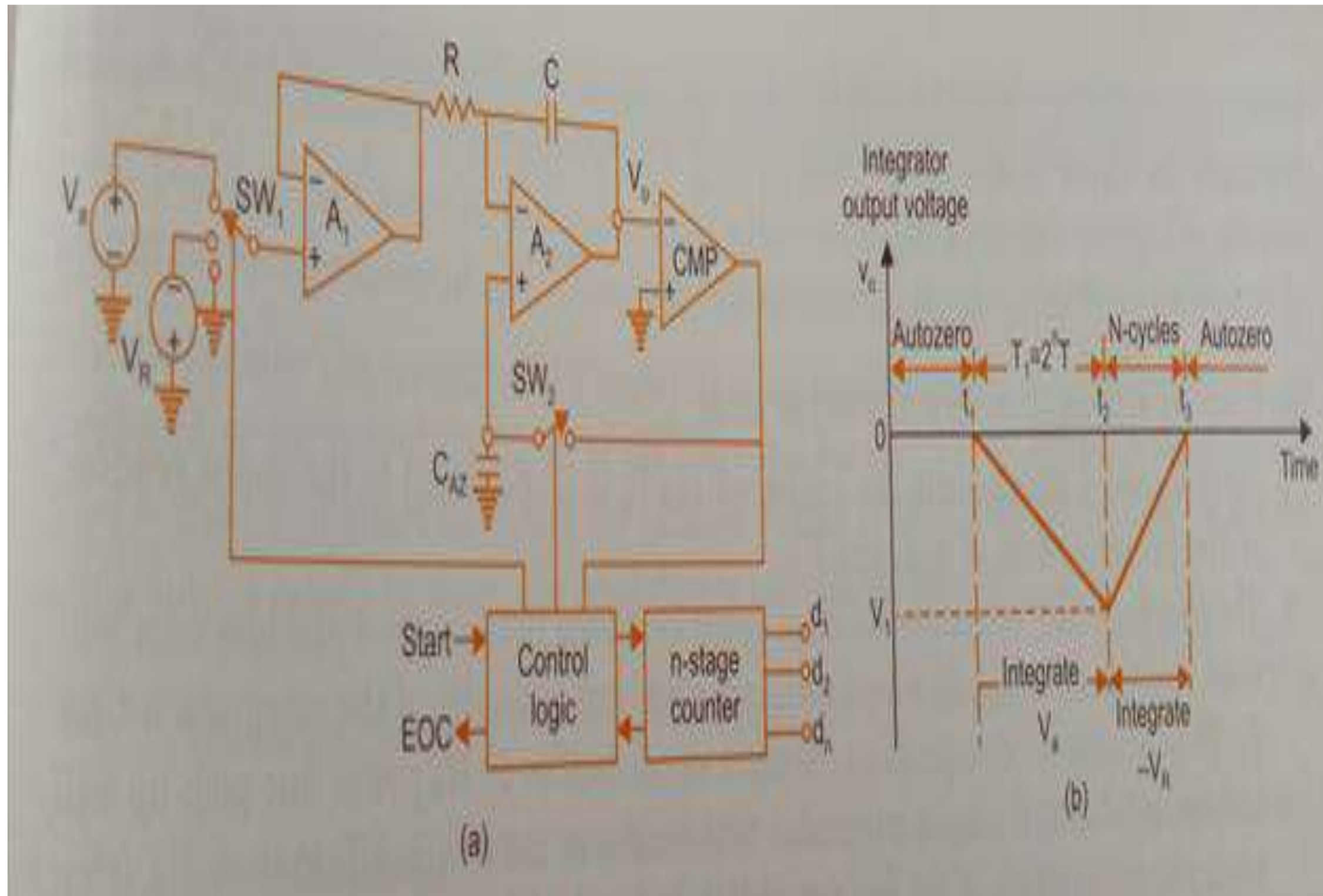


- Later when SW2 opens, CAZ acts as a memory to hold the voltages required to keep the offset nulled
- At the arrival of the START command at $t=t_1$, the control logic opens SW2 and connects to V_a and enables the counter starting from zero
- The circuit uses an n -stage ripple counter and therefore the counter resets to zero after counting 2^n pulses
- The analog voltage V_a is integrated for a fixed number 2^n counts of clk pulses after which the counter resets to zero. If the clock period is T the integration take place for a time $T=2^n \times T$ and the output is a ramp going downwards
- The counter resets itself to zero at the end of the integral T_1 and the switch SW1 is connected to the reference voltage $-V_R$
- The output voltage V_o will now have a +ive slope. As long as V_o is -ive, the output of the comparator is +ive and the control logic allows the clock pulse to be counted
- When V_o become just zero at time $t=t_3$, the control logic issues an end of conversion (EOC) command and no further clock pulses enter the counter.





Dual Slope Type - ADC





Dual Slope Type - ADC



$$T1=t2-t1=2n\text{countsclock rate}$$

$$t3-t2=\text{digital count } N\text{clock rate}$$

$$\text{For an integrator, } \Delta V_o = (-1/RC) V(\Delta t)$$

Voltage V_o will be equal to V_1 at the instant t_2 and can be given as

$$V_1 = (-1/RC) V_a(t_2 - t_1)$$

The voltage V_1 is also given by

$$V_1 = (-1/RC)(-V_R)(t_2 - t_3)$$

$$\text{so, } V_a(t_2 - t_1) = V_R(t_3 - t_2)$$

$$\text{sub } t_2 - t_1 = 2n \text{ \& } t_3 - t_2 = N$$

$$V_a(2n) = V_R(N)$$

$$V_a = V_R(N/2n)$$





Features of Single Slope and Dual Slope Converters



- **Comparison with Reference Voltage:** Both single and dual slope converters compare the unknown analog input voltage with a reference voltage. The reference voltage starts from 0V and increases linearly over time.
- **Ramp Generation:** A ramp generator, often in the form of an integrator or DAC, generates the linearly increasing reference voltage. This ramp continues to rise until it matches the input voltage.
- **Time Proportionality:** The time taken for the ramp voltage to reach the input voltage is proportional to the amplitude of the input voltage.
- **Digital Counter:** A digital counter measures the time period during which the ramp voltage is lower than the input voltage.





Advantages of Single Slope and Dual Slope Converters



- **High Accuracy:** The integration process allows for a high degree of accuracy in measuring the input voltage, making it suitable for applications requiring precise measurements
- **Wide Input Range:** This type of ADC can handle a broad range of input voltages, accommodating various applications
- **Low Noise Sensitivity:** The integration process helps average out noise, improving the overall signal quality and measurement reliability.





Disadvantages of Single Slope and Dual Slope Converters



- **Clock Drift:** Variations in the clock frequency can introduce errors, leading to inaccurate conversion results.
- **Component Sensitivity:** Errors can occur due to variations in component values, such as resistors and capacitors, which may drift over time or with temperature changes.
- **Temperature Effects:** The values of the capacitance and resistance in the ramp generator circuit can change with temperature, affecting the accuracy of the integrated output. These changes can cause variations in the slope of the ramp signal, leading to inconsistent conversion times for the same input.
- **Calibration Drift:** Over time, the system may require recalibration due to component aging, clock drift, or temperature-induced variations, leading to inaccuracies in the conversion process.
- **Speed Limitations:** Single-Slope Integrating ADCs tend to be slower compared to other types, such as flash ADCs, due to the time required for the integration and comparison processes.





Applications of Single Slope and Dual Slope Converters



- In devices that require accurate measurement of physical quantities such as temperature, pressure, and light intensity
- It is used in systems where analog signals need to be converted to digital for processing and analysis
- Employed in medical monitoring equipment to convert physiological signals into digital data for analysis and display
- Found in devices that require analog-to-digital conversion, such as digital cameras and audio equipment





THANK YOU