SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

23ECB202 – LINEAR INTEGERATED CIRCUITS

II YEAR/ III SEMESTER

1

UNIT 4 – ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTER

TOPIC 4.9 – Switches for D/A converters, high speed sample-and-hold circuits

Switches For DAC

- The Switches which connects the digital binary input to the nodes of a D/A converter is an electronic switch.
- Although switches can be made of using diodes, bipolar junction Transistors, Field Effect transistors or MOSFETs, there are four main configurations used as switches for DACs.

They are

i) Switches using overdriven Emitter Followers.

ii) Switches using MOS Transistor- Totem pole MOSFET Switch and CMOS Inverter Switch.

iii) CMOS switch for Multiplying type DACs.

iv) CMOS Transmission gate switches.

These configurations are used to ensure the high speed switching operations for different types of DACs.

Switches using overdriven Emitter Followers

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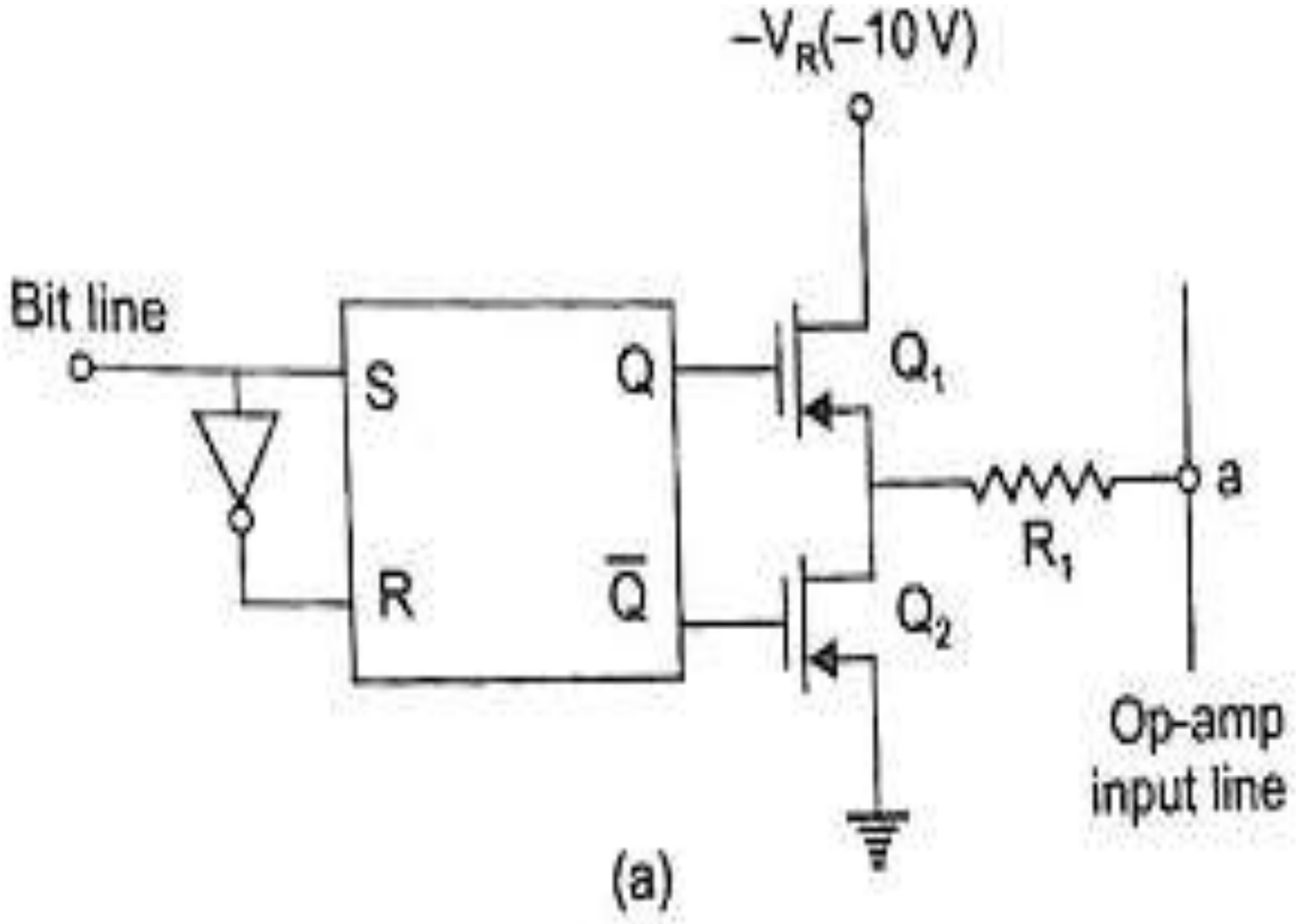
- Although switches can be made of using diodes, Bipolar junction Transistors, Field Effect transistors or MOSFETs, They are

i) Switches using MOS Transistor- Totem pole MOSFET Switch
ii) CMOS Inverter Switch.

Totem pole MOSFET Switch

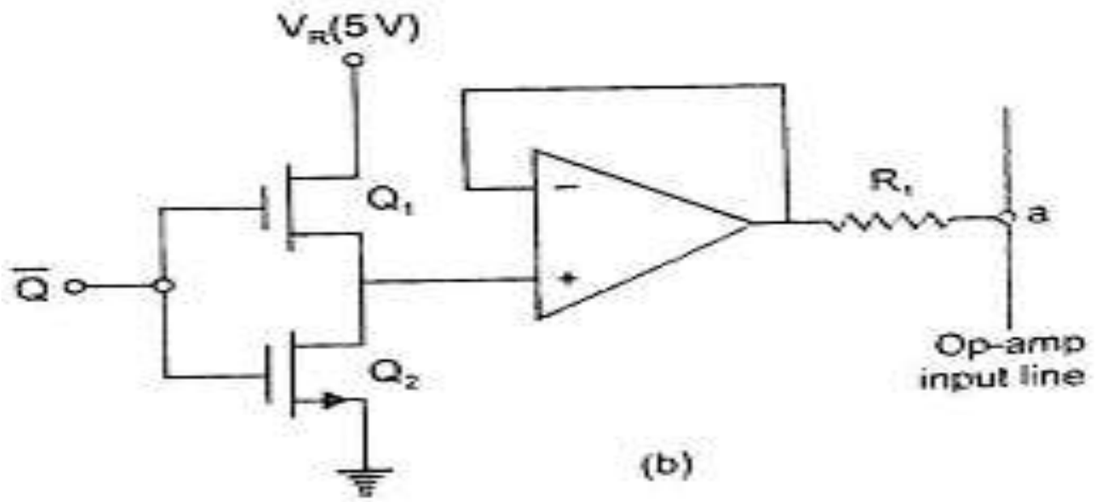
- The switches are in series with resistor R and therefore, their on resistance must be very low and they should have zero offset voltage.
- Bipolar transistor do not perform well as voltage switches, due to the inherent offset voltage when in saturation. However, using MOSFET, this can be achieved.
- Different types of digitally controlled SPDT electronics switches are available.
- A totem pole MOSFET driver feeds each resistor connected to the inverting input terminal 'a' . The two complementary gate inputs Q and ¯come from MosFET S-R flip-flop or a binary cell of a register which holds one bit of the digital information to be converted to an analog number. Assume a negative logic, i e. logic '1' corresponds to -10 V and logic "0' corresponds to zero 0v.
- If there is 'l' in the bit line, S=1 and R= 0 so that Q =1 and ¯= 0. This drives t he transistor Q1 on, thus connecting the resistor R1 to the reference voltage -VR whereas the transistor Q2 remains off. Similarly a "0" at the bit line connects the resistor R1 to the ground terminal

Switches using overdriven Emitter Followers



CMOS Inverter Switch

- Another SPDT switch consists of CMOS inverter feeding an op-amp voltage follower which drives R1 from a very low output resistance.
- The circuit is using a positive logic with V(1) = VR =+5 V and V(0)= 0 V. The complement ¯of the bit under consideration is applied at the input.
- Thus ¯=0 makes transistor Q1 off and Q2 on. The output of the CMOS inverter is at logie 1, that is, 5 V is applied to resistor R1 through the voltage follower. And if ¯= 1 the output of the CMOS inverter is 0 V connecting the resistance R1 to ground



High Speed Sample and Hold Circuits

- Sample-and-hold (S/H) is an important analog building block with many applications, including analog-to-digital converters (ADCs) and switched-capacitor filters.
- The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing.
- Taking advantages of the excellent properties of MOS capacitors and switches, traditional switched capacitor techniques can be used to realize different S/H circuits [1].
- The simplest S/H circuit in MOS technology is shown in Figure 1, where *Vin* is the input signal, M1 is an MOS transistor operating as the sampling switch, Ch is the hold capacitor, ck is the clock signal, and Vout is the resulting sample-and-hold output signal.
- As depicted by Figure 4. , in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor.
- The operation of this circuit is very straightforward

High Speed Sample and Hold Circuits

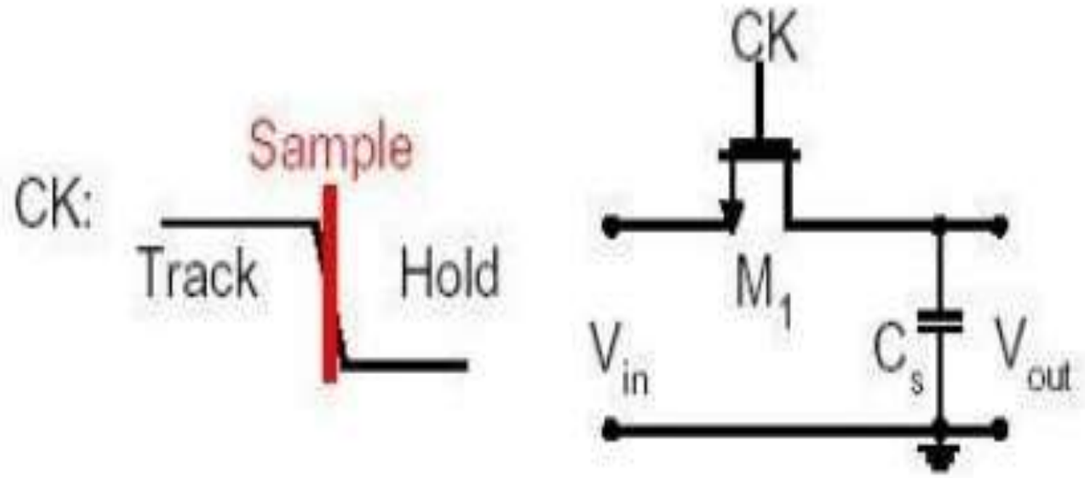


Figure 4.7 Simplest sample-and-hold circuits in MOS technology.

High Speed Sample and Hold Circuits

- A S/H circuit can be achieved using only one MOS transistor and one capacitor.
- The operation of this circuit is very straightforward. Whenever *ck* is high, the MOS switch is on, which in turn allows *Vout* to track *Vin*.
- On the other hand, when *ck* is low, the MOS switch is off. During this time, *Ch* will keep *Vout* equal to the value of *Vin* at the instance when *ck* goes low.
- Unfortunately, in reality, the performance of this S/H circuit is not as ideal as described above.
- The two major types of errors occur. They are charge injection and clock feed through, that are associated with this S/H implementation.
- Three new S/H techniques, all of which try to minimize the errors caused by charge injection and/or clock feed through.

THANK YOU